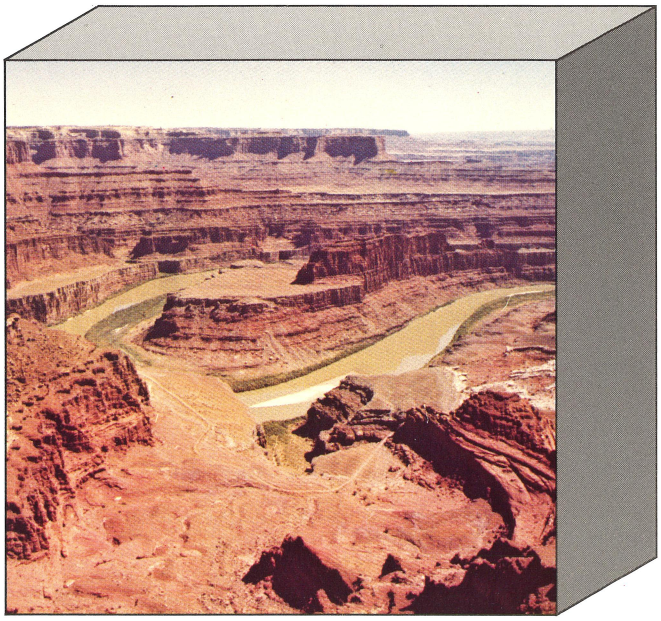
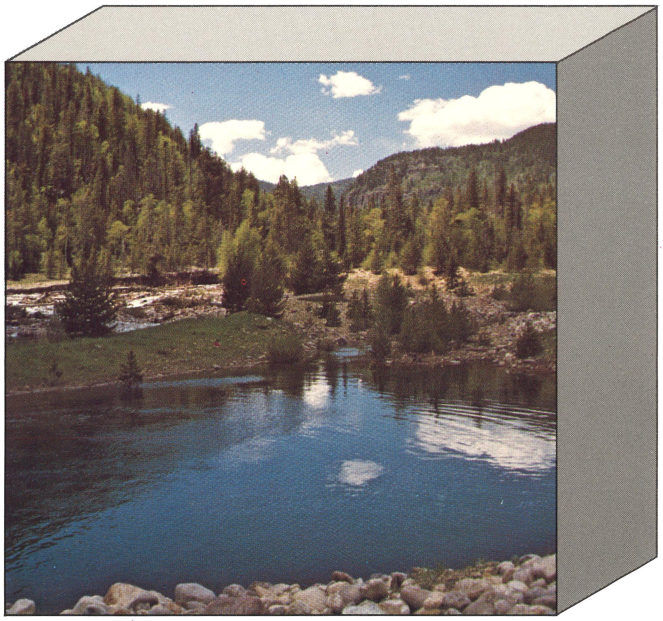
University of Utah

Department of Computer Science

Major Research Projects





Research activities in the Department of Computer Science at the University of Utah cover a wide spectrum of areas in computer science. In this brochure, the larger projects in the department are described. Brief profiles of the department, the University and the surrounding Utah area are also given.

Further information about these research projects or the department can be obtained by writing to:

Department of Computer Science
University of Utah
Salt Lake City, Utah 84112

11

Applicative Multiprocessing Systems

Faculty

Robert M. Keller
Gary Lindstrom
Suhas Patil

Staff

2 PhD Students
1 MS Student
1 Undergraduate
1 part-time Programmer

Nature of the Work

This project supports research on the design and exploitation of distributed computer systems which support applicative (e.g. function-based and data-flow) languages. Current activity is centered around the preliminary design of a multiprocessing system called AMPS, which supports a version of LISP as its machine language, in a mode of evaluation which is primarily demand-driven. A spin-off from this work is an investigation of the use of applicative languages and their graphical representation for the design automation of VLSI components.

Current Work Areas

- Exploration of applicative programming techniques for succinct specification of problem solutions, especially in problems which can exploit conceptually infinite data structures, such as simulation and numerous problems in symbolic computation.
- Evaluation of load-balancing and communication network performance via simulation programs.
- Developing techniques for specifying and proving correctness of the type of evaluator used in AMPS.
- Investigation of storage reclamation techniques, e.g. multi-level reference counting.
- Investigation of alternate implementations of data structures which yield greater concurrency.
- Investigation of resource control primitives in an applicative programming setting.

Selected Results

Representative publications are:

R. M. Keller, G. Lindstrom, and S. Patil; "A loosely-coupled applicative multi-processing system"; AFIPS Proc. 613–622 (June 1979).

A. K. Nori; "A storage reclamation scheme for Applicative Multiprocessing System (AMPS)"; M. S. Thesis (Oct. 1979).

R. M. Keller, G. Lindstrom, and S. Patil; "Data-flow concepts for hardware design"; Proc. Compcon (Feb. 1980).

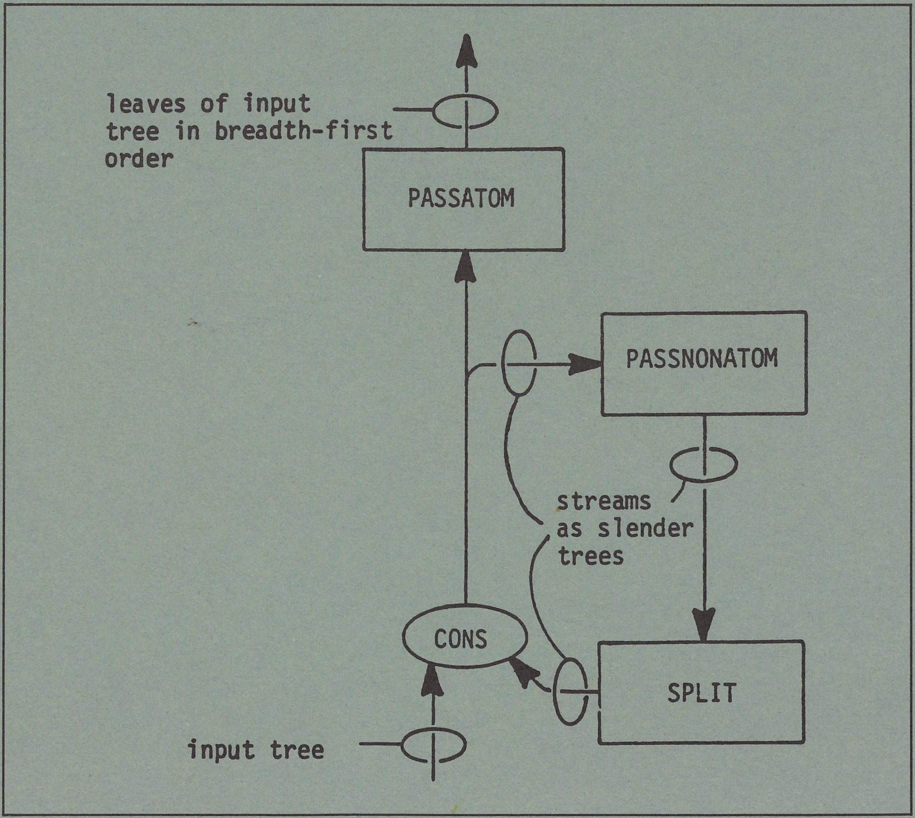
Facilities

Currently a simulator is used to perform a primitive simulation of the AMPS evaluation scheme, giving some measures of expected performance in a multiprocessor setting and much feedback about the relationship between programming style and concurrency. A compiler translates a LISP-based language into the machine language for input to this simulator. A second simulator has been developed which uses a synthetic load to drive a model of the communication network. Further software of this type is under development on the department's DECSYSTEM 2060.

Support

Current support is through two NFS grants:

- Asynchronous Computation
- Higher-Level Control Description in Programming Languages.



2

Computer Aided Geometric Design and Computer Graphics

Faculty

Richard F. Riesenfeld
Robert E. Barnhill

Staff

3 PhD Students
4 MS Students
2 Scientists from local industry

Nature of the Work

This group is concerned primarily with the representation and manipulation of free-form geometry models in a computer, as well as the generation of synthetic images based on these models. The activities associated with this project draw on many varied disciplines including aspects of modelling theory, approximation theory, numerical analysis, interactive computer graphics, programming language development, and industrial design and manufacturing. The results of this kind of research have applications ranging from computer animation to aircraft and telephone handset design.

Current Work Areas

The CAGD Group is currently interested in a wide range of topics, including:

- CAGD systems
- Computer graphics techniques
- High quality images in the context of CAGD
- Subdivision techniques for CAGD and graphics
- Discrete splines in CAGD and graphics
- CAGD specification languages
- Nontensor product models for CAGD
- Techniques for unifying geometry, analysis, and graphics

Selected Results

This group has published results which have contributed to advancing the theory, the applications, and the fundamental ways of viewing problems in CAGD. The group developed the B-spline method of curve and surface design, which is well known and commonly used throughout the world. Other advances involve the use of symbolic processing to support high level expressions for surface definition schemes, and the use of the theory of total positivity to increase the understanding and utility of variation diminishing methods for curve and surface design. Lately the group has been exploring the implications of a new theory of subdivision based on discrete splines, especially in its utility for providing a central core routine of a major CAGD System called Alpha 1. Representative publications are:

Barnhill, R. E. and Riesenfeld, R. F. (Editors); *Computer Aided Geometric Design*; Academic Press (1974).

E. Cohen, T. Lyche, and R. F. Riesenfeld; "An Application of Discrete B-splines and Subdivision Techniques in Computer Aided Geometric Design and Computer Graphics"; To appear in Computer Graphics and Image Processing (1980).

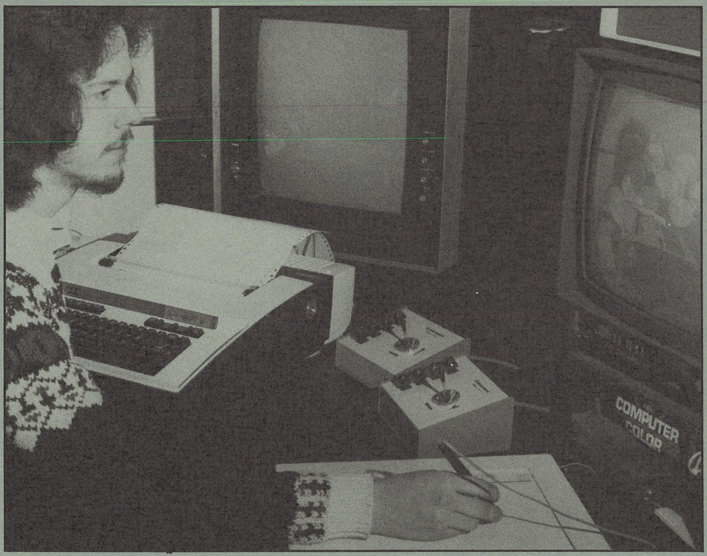
J. M. Lane and R. F. Riesenfeld; "A Theoretical Development for the Computer Generation and Display of Piecewise Polynomial Surfaces"; IEEE Trans on Pattern Analysis and Machine Intelligence (Jan. 1980).

Facilities

The main graphics facility, an Evans & Sutherland Picture System and a Grinnell Frame Buffer, is supported by a PDP–11 and connected to the main DECSYSTEM 2060 via a high speed, dual ported disk. We are currently seeking means for upgrading and adding to all of this equipment. There is also a photo lab and photographic engineer available for film processing of computer generated images.

Support

The project has been principally funded by the NSF, whose support for this work has been continuous since 1973. It has also received minor support from the ONR and the private sector.



3

Data-Driven Research Project

Faculty

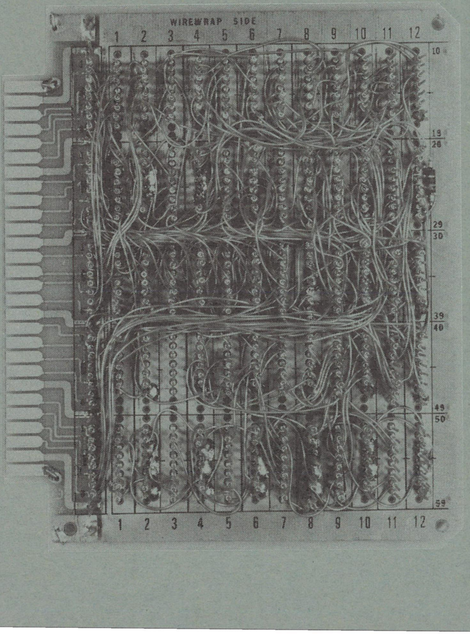
A. L. Davis

Staff

4 graduate students
3 senior technical staff
1 technical manager
2 junior technical staff
4 part time student employees

Nature of the Work

The DDRP (Data-driven research project) is a machine organization project which is investigating the organization of highly concurrent digital systems. The project is concerned with programming languages and models, concurrent machine architecture, concurrent programming methodology, and practical issues involving the construction of concurrent systems. The current research effort is centered around the dataflow or data-driven program model, which allows programs containing very high levels of concurrency to be represented. The DDRP has designed a recursive architecture of processing modules which will support the concurrent execution of data-driven programs. A module of this architecture (known as DDM1 for data-driven machine #1) has been constructed and is currently operational. The machine language of DDM1 is a particular data-driven program schema known as data-driven nets (DDN's). A successor machine (DDM2) has been designed and is almost operational. The main improvement is that DDM2 is capable of doing operations on atomic data structures which are generalized tree structures. The DDN schema is a graph and a system exists for drawing DDN programs, rather than using statement languages which are felt to be poor conceptual aids in a concurrent environment.



Current Work Areas

- Investigation and construction of graphical programming aids.
- Investigation of arbitrary precision arithmetic schemes.
- Automatic decentralized resource allocation methods.
- Evaluation and modification of the existing DDM1 and DDM2 systems.
- Application studies for data-driven systems in general.
- Investigation of high level language structures for concurrent programming.
- Investigation of several circuit switching structures for multi-processing.
- Decentralized control parallel architecture studies.
- Self managing storage system research.

Selected Results

Representative publications are:

Davis, A.; ''The Architecture and System Method of DDM1: A Recursively Structured Data-Driven Machine''; Proceedings of the Fifth Annual Symposium on Computer Architecture (1978).

Davis, A.; ''DDN's—A Low-Level Program Schema for Fully Distributed Systems''; Proceedings of the First European Conference on Parallel and Distributed Processing, Toulouse (Feb. 1979).

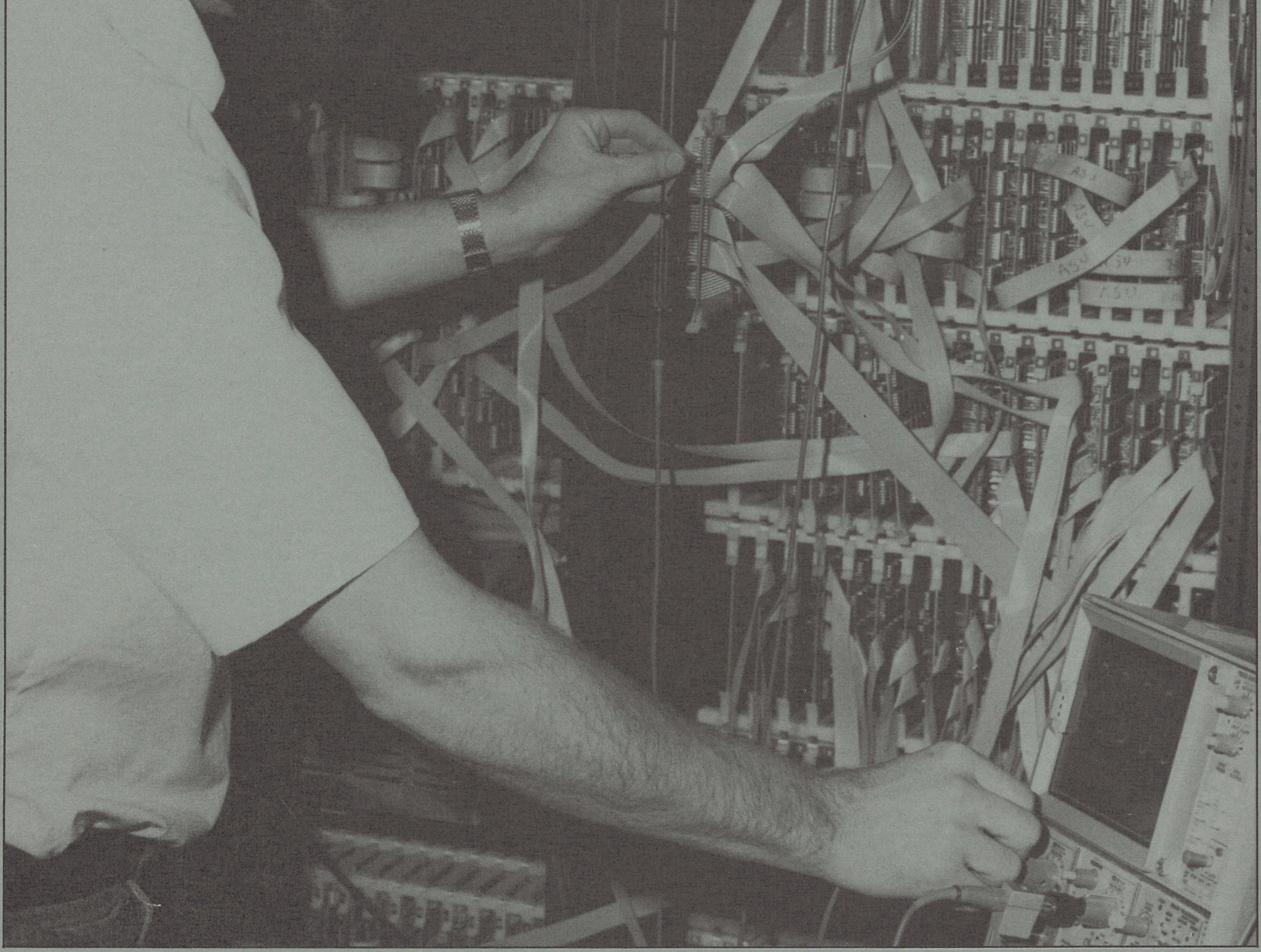
Davis, A.; ''A Data-Flow Evaluation System Based on the Concept of Recursive Locality''; Proceedings NCC '79, New York (1979).

Facilities

DDRP resources include the use of the department's DECSYSTEM 2060 facility with the usual complement of terminals. Special DDRP resources include a complete hardware prototype laboratory, the DDM1 and DDM2 prototype systems, a Tektronix storage tube graphics terminal, a Megatek 7000 refresh graphics system, a PDP–11/34, a graphical hard copy device, a 4 bit CDL color frame buffer, and a selection of hardware test equipment.

Support

The DDRP is supported by a grant from the Burroughs Corporation.



4

Digital Signal Processing and Sensory Information Processing

Faculty

Steven F. Boll
Craig Rushforth (EE)
Brent Baxter
Thomas G. Stockham (*)
Ercolino Ferretti
Lamar Timothy (EE)
Elaine Cohen

Staff

3 Professional Staff
10 Graduate Students
3 Lab Technicians

Nature of the Work

The SIP group is involved in both fundamental and applied research in digital signal processing. Fundamental work centers on development of sensory perception models and mathematical methods to support computer implementation of these models. Applications include enhancement of actual audio signals by removing noise contamination, speech analysis-synthesis, bandwidth compression, generation of high quality synthetic audio, digital computer music generation, restoration of atmospherically degraded astronomical images, perceptual models of the human visual system, and related topics.

Current Work Areas

Development of algorithms for:

- The study of distant dim stellar objects, especially distant binary star systems, with the restoration technique developed by the SIP group.
- The suppression of acoustic noise in speech.
- Audio bandwidth compression using linear predictive coding and short-time spectral analysis.
- The perceptual modeling of vision and hearing using the recently developed "Constant-Q" transform.
- Speech and image enhancement through deconvolution and super-resolution.
- The development of high quality music synthesis tools.

Selected Results

The following is a list of some applications of the work completed by the SIP group:

- Incorporation by the U.S. Navy of an algorithm developed at Utah for noise suppression in their digital voice communication terminal to be used throughout the Department of Defense.
- Practical isolated word recognition and word spotting systems with better than 95% accuracy.
- The SIP group has recently shown that by removing the effects of atmosphere turbulence, spatial (angular) resolution can be improved on the 4 meter Kitt Peak telescope by a factor of 40 to the so-called diffraction limit. A further four fold increase in resolution has been shown to be possible by means of super resolution techniques. This work has resulted in the first known high resolution image of the binary star Capella.

Representative publications are:

Boll, S. E.; "Suppression of Acoustic Noise on Speech using Spectral Subtraction"; IEEE Transactions on Acoustics, Speech, and Signal Processing; Vol. ASSP–27, No. 2 (April 1979).

Frost, R. L., Rushforth, C. K., and Baxter, B. S.; "A Fast FFT based Algorithm for Least Squares Phase Estimation in Speckle Imaging"; Applied Optics, Vol. 18, No. 12, pp. 2056–2061 (June 1979).

Christiansen, R. W. and Rushforth, C. K.; "Detecting and Locating Key Words in Continuous Speech using Linear Predictive Coding"; IEEE Transactions on Acoustics, Speech, and Signal Processing; Vol. ASSP–25 (October 1977).

Stockham, T. G.; "Image processing in the context of a visual model"; IEEE Proceedings, pp. 828–842 (July 1972).

Facilities

As part of a dedicated SIP group computing facility, the group has a PDP–10, PDP–11/45, FPS–120B Array Processor, and high precision digital recording and playback equipment for both sound and images. The group has an acoustically shielded sound laboratory, an extensive signal processing software library, and computer music generation software systems.

Support

The SIP group is currently supported by grants from the Information Processing Techniques Office of the Defense Advanced Research Projects Agency, and the Air Force Office of Scientific Research.

---

*Professor Stockham is currently in residence at Soundstream Corporation.

5

Medical Image Processing

Faculty

Brent Baxter
James Sorenson (Radiology)
Robert Anderson (Radiology)

Staff

4 Graduate Students
1 Staff programmer
1 part-time technical manager

Nature of the Work

The project is evaluating a new viewing device that allows a physician to examine multiple parallel CT scan sections simultaneously in their proper orientation in all three dimensions. Clinical and phantom images studied on this device have shown that certain anatomical features important in scan interpretation are more easily appreciated when viewed in 3-D. A 3-D line drawing graphics capability is being developed for the viewer to be used in direct guidance of surgical instruments during tumor biopsy and other invasive procedures in the brain. Other work is directed at developing and evaluating improved methods for displaying nuclear medicine images, and for processing chest radiographs to increase tumor detectability.

Current Work Areas

- 3-D viewer construction and testing.
- Effective use of the 3-D line drawing capability.
- Evaluation of improved nuclear medicine display systems.
- Evaluation of scatter reduction in chest radiography.

Selected Results

Early results include the discovery that the human visual system seems to fill in smoothly between virtual image planes displaced in depth. Certain anatomical and pathological structures important in cancer detection are more readily appreciated when viewed on the 3-D viewer than when seen on conventional planar imaging systems such as TV or film. Representative publications are:

Lee, T. G. et al; ''Potential Applications For Three Dimensional Display of Ultrasound Images''; presented at 2nd Meeting of the World Federation of Ultrasound in Medicine and Biology, Miyazaki, Japan (July 1979).

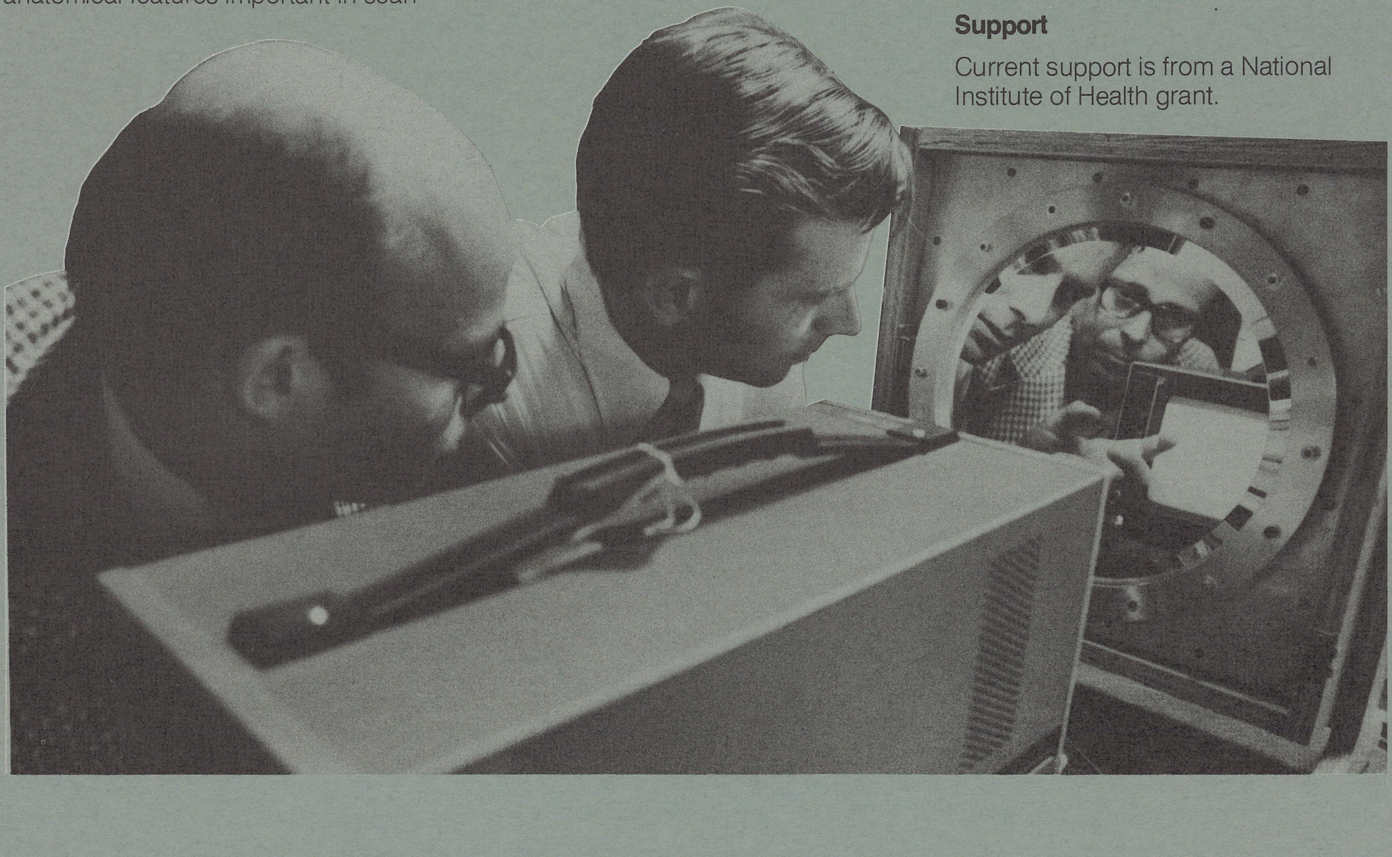
Baxter, B.S.; ''Precision Computer Display Techniques in Nuclear Medicine''; Proc. SPIE, San Diego (August 1979).

Facilities

The medical image processing group has X-ray equipment, a multiuser Eclipse computer equipped for image processing, an automatic film processor, and a 3-D viewing apparatus.

Support

Current support is from a National Institute of Health grant.



6

Small Computer Project

Faculty

Martin L. Griss
A. L. Davis
Anthony C. Hearn

Staff

3 graduate students
2 undergraduate students
1 technician

Nature of the Work

The project activities are centered around a newly evolving departmental Small Computer Laboratory. The group is currently investigating techniques for system portability, the development of personalized algebra machines, LISP implementation strategies on small machines, and multi-microprocessor system software. The primary goal of the group is to produce working and useful software tools which will support these efforts.

Current Work Areas

- Software portability strategies for small machines
- Network interconnections and software
- Small machine LISP and algebra systems
- Multiprocessor dataflow simulation software
- Architecture and hardware augmentation for symbol manipulation

Selected Results

Early results of this project include the development of two portable languages for small machines, used to implement system software (editor, file transfer program), and LISP systems for a variety of small computers. A general purpose assembler generator has been written in one of the languages. Published results can be found in:

Griss, M. L.; "BIL: A Portable Implementation Language for LISP-like Systems"; Utah Symbolic Computation Group, Operating Note No. 36, (1977).

Griss, M. L., R. R. Kessler, and G. Q. Maguire, Jr.; "TLISP—A 'Transportable' LISP Implemented in P-code"; Proc. EUROSAM 79, Springer-Verlag, New York, 491–502 (1979).

Byard, R. P.; "A Portable Assembler Writing Kit"; M. S. Thesis, Department of Computer Science, University of Utah, (March 1979).

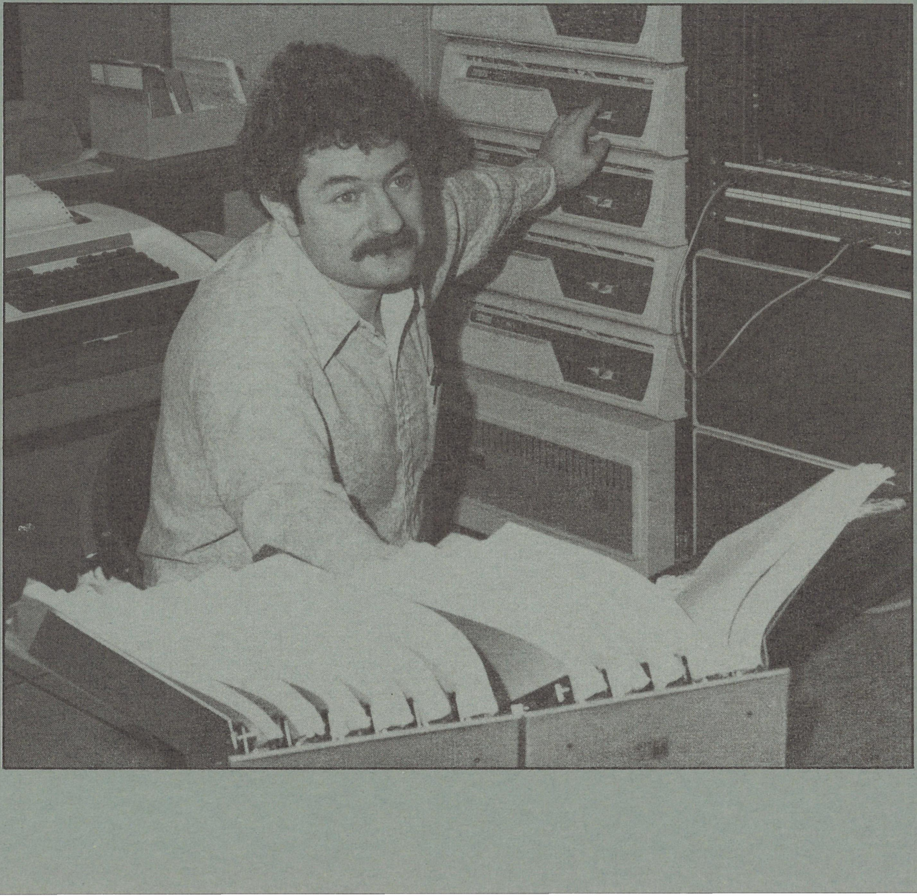
Wampler, B. E.; "LS2: A Portable Programming Language"; Proceedings of the Second Rocky Mountain Symposium on Micro Computers, (August 1978).

Facilities

The Small Computer Laboratory currently has a PDP–11/34, 4 PDP–11/04s, 2 printers, an 80Mb disk, a variety of terminals, and 4 micro-computers with dual floppy disks (using Z80, 8080 and M6800 micro-processors), and a single board iSBC 8086 micro-computer. There are facilities for interconnecting the machines in a variety of ways, and with the departmental DECSYSTEM 2060.

Support

The major support aimed directly at this project has been an NSF Research Equipment Grant, which has permitted the establishment of the Small Computer Laboratory. Industrial gifts have also added additional equipment to the Laboratory. The actual research has been supported as part of the work of the Symbolic Computation Group and the DDRP.



7

Symbolic Computation Group

Faculty

Anthony C. Hearn
Martin L. Griss

Staff

2 Post Doctoral Fellows
1 Programmer
3 PhD Students
3 MS Students

Nature of the Work

The research of the Symbolic Computation Group is directed towards the design and development of high quality symbol manipulation programs used for computer algebra, program transformations, and experimental language systems. Areas of study include algorithm development, experimental implementation and evaluation of LISP based and LISP like systems, compilers, facilities for improving LISP programming environments and microprogrammed systems.

Current Work Areas

The group is currently interested in a wide range of topics, including:

- Algebraic manipulation
- Software portability
- Compiler writing systems
- Innovative symbol manipulation methods (hashing, pattern matching, etc.)
- LISP system implementation
- Small machine LISP and algebra systems
- Mode based LISP and algebra systems
- LISP and algebra machines

Selected Results

The most well known program developed by this group is the REDUCE computer algebra system, which is widely available throughout the world and has been used in several hundred published calculations. Concern with portability and robustness has made it possible to provide this software on a variety of different computers, including the IBM 360 and 370 series, DECSYSTEMS 10 and 20, Univac 1100 series, CDC 6000's and 7000's, Burroughs B6000's and B7000's, and the Cray-1. The group has also published a standard for a portable LISP (Standard LISP), and developed a LISP compiler to support this standard, which may be implemented on a wide variety of computers. A number of other systems, including a microcoded LISP and REDUCE system on a Burroughs B1800 computer, a META/REDUCE compiler writing system, and other experimental languages have been described in published articles, and distributed. Representative publications are:

Marti, J., A. C. Hearn, M. L. Griss and C. Griss; ''Standard LISP Report''; SIGPLAN Notices 14, No. 10, 48-68 (1979).

Griss, M. L. and A. C. Hearn; ''A Portable LISP Compiler''; Software—Practice and Experience (to appear).

Hearn, A. C., and A. C. Norman; ''A One Pass Pretty Printer''; SIGPLAN Notices, ACM, New York, 14, No. 12, 50–58 (1979).

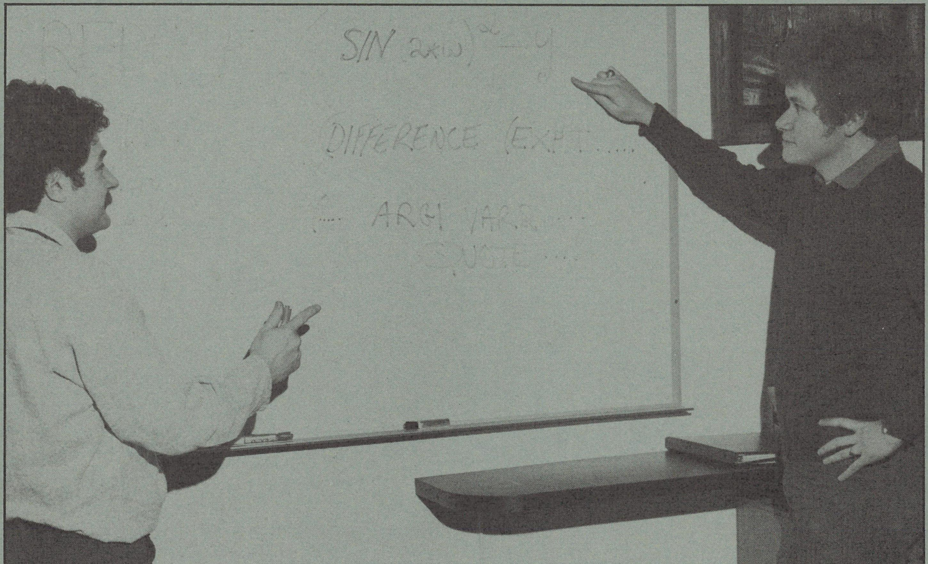
Griss, M. L. and R. R. Kessler; ''REDUCE 1700: A Microcoded Algebra System''; Proc. Micro-11, 130–138 (1978).

Facilities

Though the main computing activity of the group is centered on the department's DECSYSTEM 2060 and the Burroughs B1855, researchers in this group are able to study the portability and use of fairly large production programs on a wide range of machines by means of networking connections via the Arpanet and Telenet.

Support

The research activities of the group have been funded by a number of different agencies with the principal support coming from the NSF; significant grants have also been made by the Burroughs Corporation. Some support for a Cray-1 implementation of REDUCE has been provided by the Lawrence Livermore Laboratory.



8

Theoretical Aspects of Software Systems

Faculty

Robert M. Keller
P. A. Subrahmanyam

Staff

3 PhD Students

Nature of the Work

The group's research deals with fundamental problems confronting the software designer interested in the production of high quality software. Areas of concern are automatic synthesis of abstract data type and synchronizer realizations, the verification of such realizations, and the semantics of programs, including concurrent programs. Although the group has a theoretical orientation, practical and human-engineering aspects play an important role as motivations requiring new theoretical insights.

Current Work Areas

- Development of a theory of program synthesis using an algebraic framework for semantics of program specification.
- Automating the implementation of abstract data types and the proofs of such implementations.
- Use of temporal logic for specification and automatic implementation of synchronizers.
- Use of the Stanford Verifier for proving correctness of sentinels, a highly flexible, yet semantically transparent synchronizer construct.
- Development of modeling and proof techniques for dealing with the phenomenon of indeterminacy in concurrent programs.

Selected Results

Representative publications are:

R. M. Keller; "Denotational models for parallel programs with indeterminate operators"; In E. J. Neuhold (ed.), Formal description of programming concepts, 337–366, North-Holland (1978).

R. M. Keller; "Proof methods for concurrent programs"; 654–658 of P. Wegner (ed.), Research directions in software technology, MIT Press (1979).

R. M. Keller; "Sentinels: A concept for multiprocess coordination"; University of Utah, Dept. of Computer Science, Tech. Rept. UUCS-78-104 (June 1978).

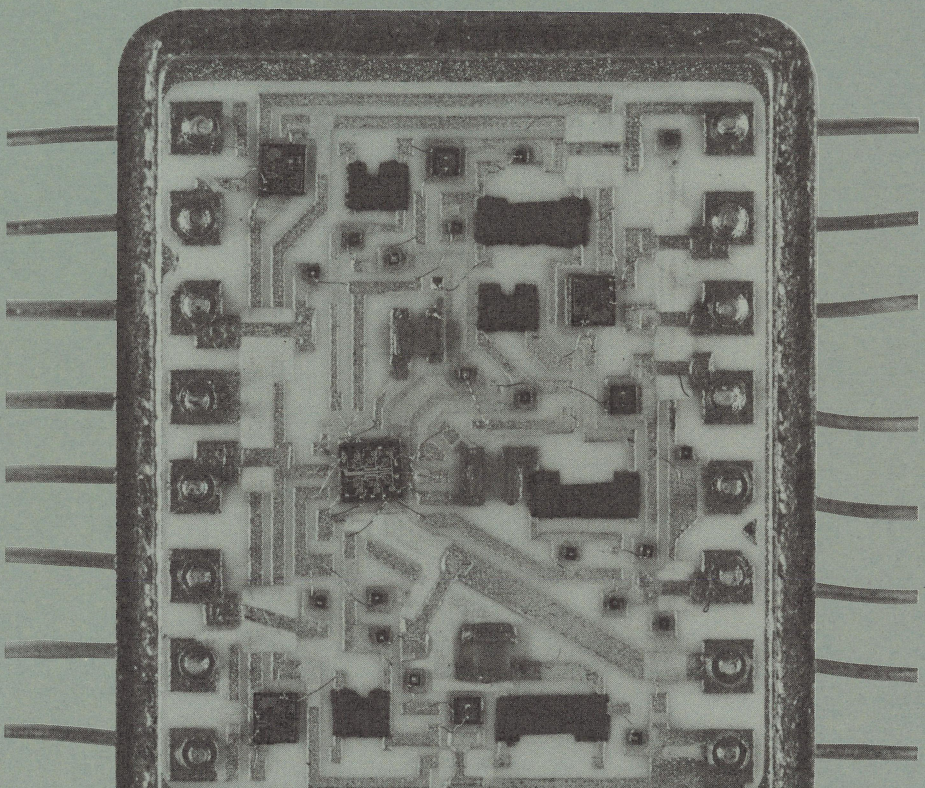
P. A. Subrahmanyam; "Towards a theory of Program Synthesis: Automating Implementations of Abstract Data Types"; Ph.D. Thesis, Department of Computer Science, State University of New York at Stony Brook (August 1979).

P. A. Subrahmanyam; "On the Word Problem for Heterogeneous Algebras"; Proc. Sixth Johns Hopkins Conference on Information and System Sciences (March 1979).

P. A. Subrahmanyam; "Interprocess communication and Blockage Propagation in Multi-Processor Configurations"; Proc. of the 11th Hawaii Intl. Conf. on Inf. and System Sciences (January 1979).

Support

Support is through an NSF grant on Asynchronous Computation.



9

VLSI Group

Faculty

Suhas Patil
Kent Smith
Robert Huber (EE)
Roland Ure (EE)
Gary Lindstrom

Staff

9 graduate students
3 undergraduate part time employees
2 laboratory technicians

Nature of the Work

This group is working on a design methodology for programmable logic known as Stored Logic Arrays (SLA) to be used for the design of integrated circuits. The techniques are centered around the use of a uniform structure of basic logic building blocks whose interconnections are initially uncommitted. The specification of these interconnections in the SLA and the generation of masks to actually produce the integrated circuit will be done through the use of computer aids which are in the process of being developed.

Current Work Areas

The VLSI group is developing the following software design aids:

- High level language descriptions of a system.
- Compilers to take the high level description to the SLA notation.
- Programs to automatically generate tapes to drive pattern generators to make integrated circuit masks.
- Logic simulators to verify SLA designs.
- Transient analysis programs to predict device performance.
- Programs to generate testing and diagnostic information on the finished integrated circuit.

Selected Results

A representative publication is:

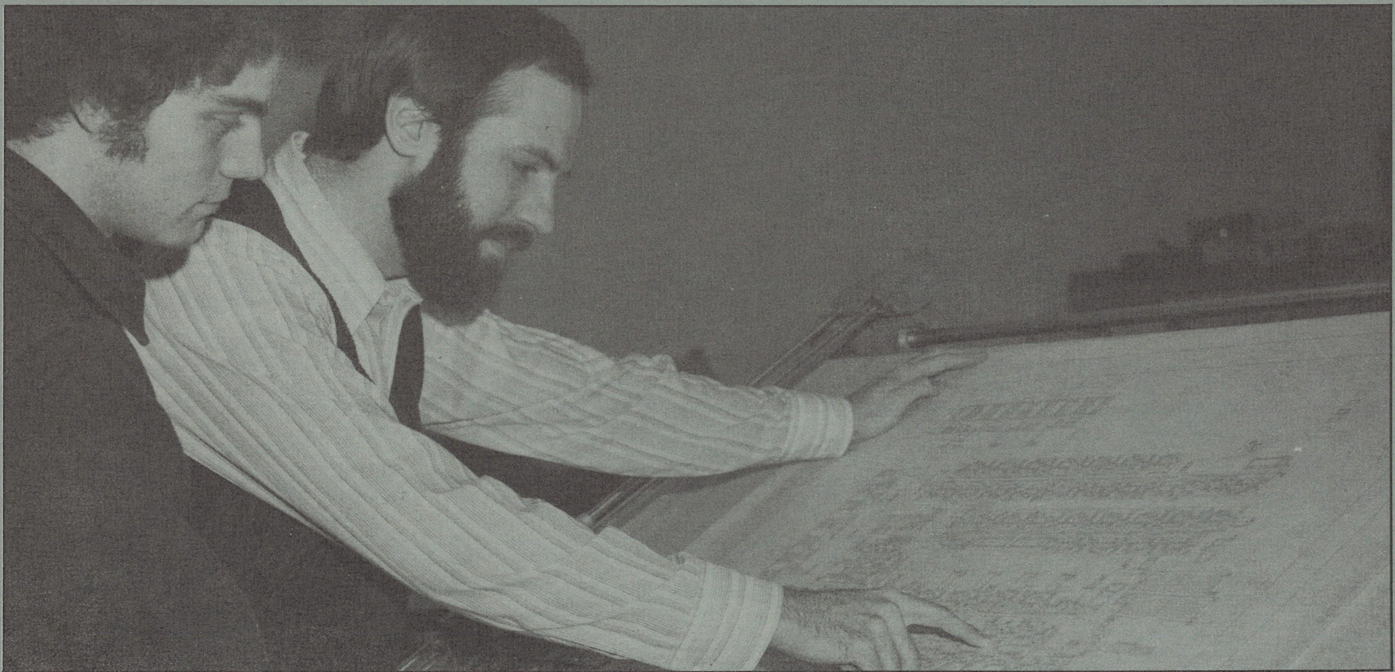
Patil, S. and Welch, T.; "A Programmable Logic Approach for VLSI"; IEEE Transactions on Computers, Vol. C-28, (Sept. 1979) pp. 594–601.

Facilities

The VLSI group uses the department's DECSYSTEM 2060 which supports SPICE2.E (A CAD transient analysis package) and SIMULOG (a logic simulation program). The group also uses the department's graphics lab to develop graphical CAD tools. A ComputerVision CAD machine has recently been donated to the University, and the group also has a 5300 square foot fabrication facility capable of producing both silicon gate NMOS and I2L circuits.

Support

The VLSI group is currently supported by a grant from NSF: "Structured Approach to VLSI Design", and by a grant from the General Instruments Corporation: "Modeling and Architecture for High Speed VLSI".



The Department of Computer Science

The Department of Computer Science offers B.S., M.E., M.S., and Ph.D. degree programs. The department currently consists of 14 regular faculty members, 10 visiting and research faculty members, 82 graduate students, and 282 undergraduate students. The undergraduate curriculum is a full 4 year program of study. The department also offers about 40 regularly scheduled graduate courses in addition to research oriented seminar courses, and the departmental colloquium series. Several of the larger research groups also hold regular group meetings where recent research work is presented. These meetings are open to all interested students and provide a regular forum for discussion and evaluation of graduate student and faculty work.

The department has an attractive complement of computing facilities, a DECSYSTEM 2060 being the main research machine. The 2060 is a site on both Arpanet and Telenet, which allows easy access to numerous other computing sites in North America and western Europe. Most offices have terminals to the DECSYSTEM 2060, and there are also several bullpen areas containing more terminals for student use. In addition, the department has a Burroughs B1855, numerous PDP-11's, several microcomputer based systems, a PDP-10, a FPS array processor, and a graphics laboratory. The graphics laboratory contains an Evans & Sutherland PS-1, a 27 bit Grinnell frame buffer, a PDP-11/34, and a dual ported disk to the DECSYSTEM 2060. Other laboratories have 3-D displays, a Megatek 7000, a CDL 4-bit color bit map display, several Tektronix storage tube displays, an electrostatic hard-copy unit, and several plotters. The department also maintains a professional photography lab, and a full-time photographer is a member of the departmental staff.

A more detailed description of the research facilities can be found in the individual research project descriptions contained in this brochure.

Faculty

Full Professors

Robert E. Barnhill, Ph.D.
Anthony C. Hearn, Ph.D.
Elliott I. Organick, Ph.D.
Thomas G. Stockham, Jr., Sc.D.
William J. Viavant, Ph.D.
Robert E. Stephenson, Ph.D.

Associate Professors

Robert M. Keller, Ph.D.
Gary E. Lindstrom, Ph.D.
Suhas S. Patil, Sc.D.
Richard F. Riesenfeld, Ph.D.

Assistant Professors

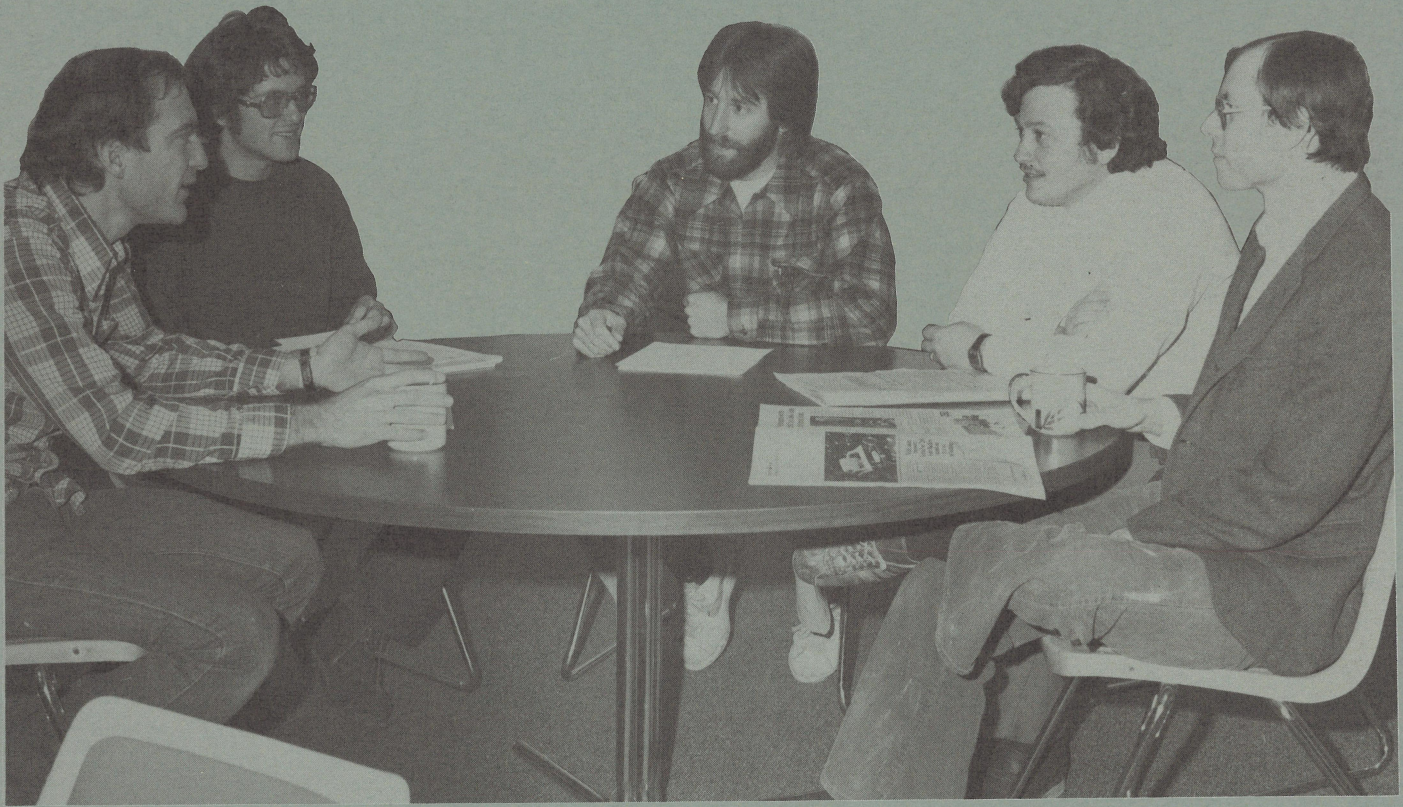
Steven F. Boll, Ph.D.
Alan L. Davis, Ph.D.
Martin L. Griss, Ph.D.
P. A. Subramahnyam, Ph.D.

Research Associate Professors

Ercolino Ferretti, B.S.
Kent F. Smith, M.S.

Research Assistant Professors

Brent S. Baxter, Ph.D.
Elaine Cohen, Ph.D.



The University of Utah

Founded in 1850, the University of Utah is the oldest state university west of the Missouri river. 22,000 students represent all 29 counties in Utah and 50 foreign countries. The 1700 member regular faculty is augmented by 1800 clinical, adjunct, research, and visiting faculty members. The University supports over 90 academic programs and offers a complete range of undergraduate and graduate degree programs in 17 colleges. The 1500 acre campus is nestled beneath the western foothills of the majestic Wasatch mountain range which borders the east side of the Salt Lake valley.

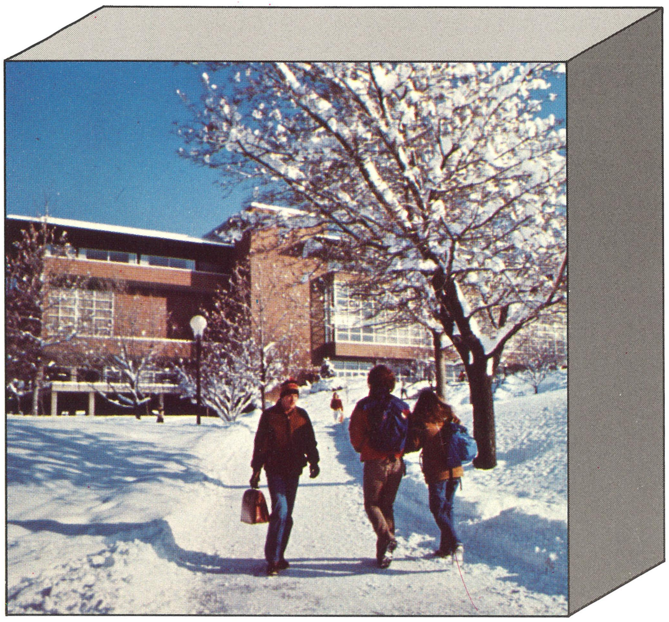
The University has numerous recreational and cultural programs which enhance student activities. The outdoor program organizes and provides instruction in mountain climbing, back packing, cross-country skiing, winter camping, white water river boating, cycling, and scuba diving. The physical education department also provides instruction in more than 80 sports. The intramural program organizes and administers a constant offering of competitive sporting events. The University also supports teams which compete on a national level in numerous sports. The ballet, music, theater, and dance departments provide continual opportunities to attend conferences, plays, readings, recitals, and concerts. There is the opportunity to participate in the types of student organizations and activities that one might expect to find in a 22,000 student university community.

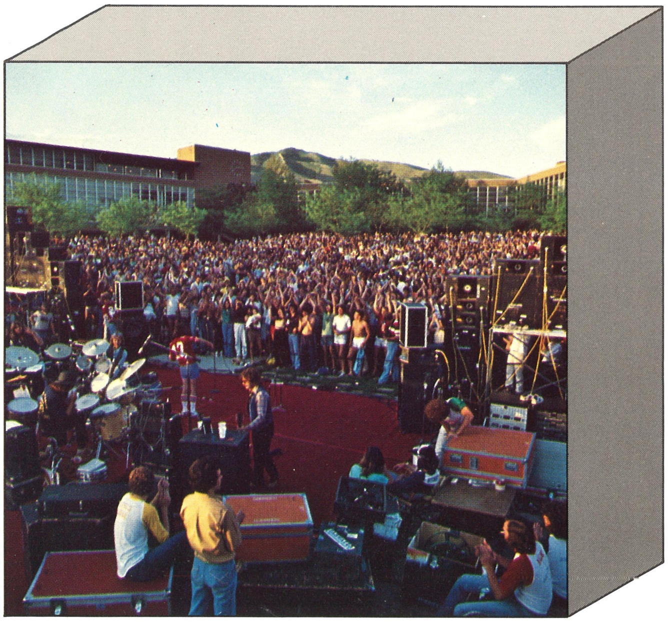
Salt Lake City

Salt Lake City is the major urban, industrial, and cultural center of the intermountain area. It is located in the northern half of Utah just east of the Great Salt Lake, and on the western edge of the Wasatch Mountain Range.

The population of the city is approximately 300,000, but the Salt Lake Valley contains about 50% of Utah's 1.3 million people. Salt Lake City provides such cultural attractions as a nationally recognized symphony orchestra and ballet company, in addition to several modern dance and theatre companies. Professional and semi-professional teams represent Salt Lake City in most major sports. Downtown Salt Lake City is 15 minutes from the Salt Lake International Airport which is served by several major air lines.

The city is almost ideally situated for rapid access to recreational opportunities. The university campus is only 30 minutes away from 6 major ski resorts which are world famous for the deep, fluffy powder snow that can only be found in an alpine desert climate. The city is located within a day's drive of 20 national parks and monuments. The massive wetlands surrounding the Great Salt Lake form one of the largest waterfowl sanctuaries in North America. These bountiful marshlands still provide a pristine opportunity to see wildlife which is no longer present in many other parts of the country. The state of Utah has long been considered a spectacular location for boating, hunting, fishing, mountain climbing, and skiing.





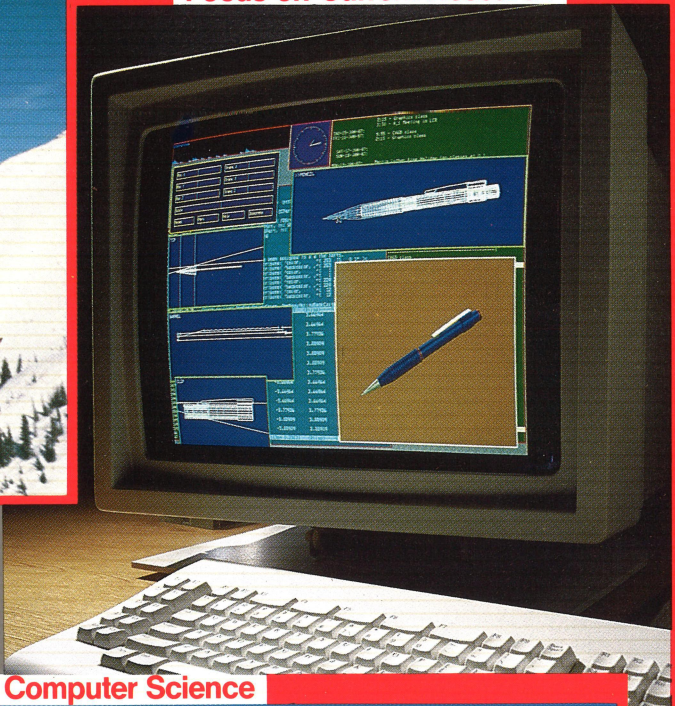
Department of Computer Science / University of Utah / Salt Lake City, Utah 84112

Telephone (801) 581-8224

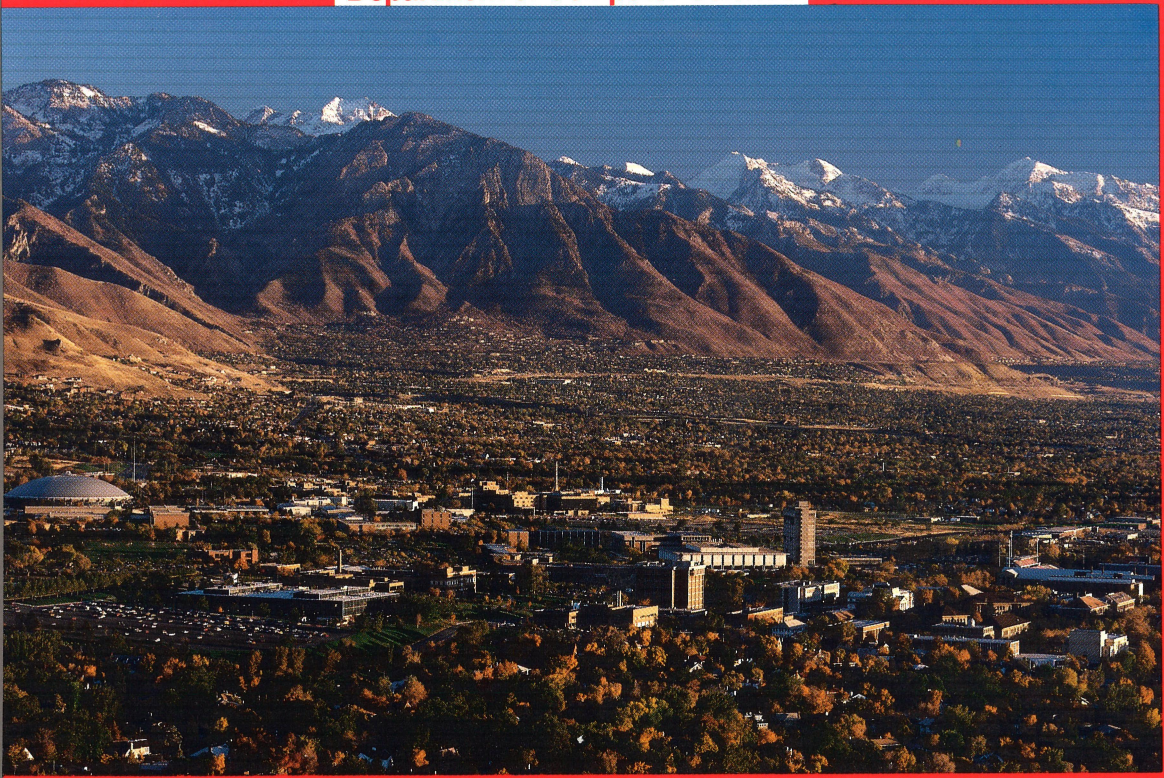
AI CAGD CAI Lisp Parallelism Robotics Text Retrieval Theory VLSI

University of Utah

Focus on Current Research



Department of Computer Science



Contents

Faculty 1
Computer Science Research Computing Facilities 2
Research Projects 5-16
CAD for VLSI Architectures 5
Computer Aided Geometric Design 6
Design and Simulation of Parallel Architectures 7
Functional Distributed Programming 8
Information-based Complexity 9
Information Retrieval and Manipulation 10
Instructional Software Systems 11
Parallel Programming 12
Portable AI Support Systems 13
Robotics and Computer Vision 15
VLSI Design Methodologies 16

Focus on Current Computer Science Research

Faculty

Chairman
Richard F. Riesenfeld, Ph.D.

Associate Chairman
Thomas C. Henderson, Ph.D.

Professors
F. Warren Burton, Ph.D.
Lee A. Hollaar, Ph.D.
Richard F. Riesenfeld, Ph.D.
Kent F. Smith, Ph.D.

Associate Professors
Elaine Cohen, Ph.D.
Thomas C. Henderson, Ph.D.
Gary E. Lindstrom, Ph.D.
Krzysztof A. Sikorski, Ph.D.

Assistant Professors
Bir Bhanu, Ph.D.
Tony M. Carter, Ph.D.
Richard Fujimoto, Ph.D.
Ganesh Gopalakrishan, Ph.D.
Spencer Thomas, Ph.D.
John Van Rosendale, Ph.D.

Research Associate Professors
Richard Brandt, Ph.D.
Ercolino Ferretti, B.Mus.

Research Assistant Professor
Robert Kessler, Ph.D.

Adjunct Professors
David C. Evans, Ph.D.
Robert M. Keller, Ph.D.
Frank Stenger, Ph.D.
Thomas G. Stockham Jr., Sc.D.
Stephen Jacobsen, Ph.D.

Adjunct Associate Professors
David Hanscom, Ph.D.
Stan Moss, Ph.D.
Tracy Peterson, Ph.D.

Adjunct Assistant Professors
Sam Drake, Ph.D.
William Salmon, Ph.D.

The Computer Science Department numbers sixteen regular, three research and eight adjunct faculty.

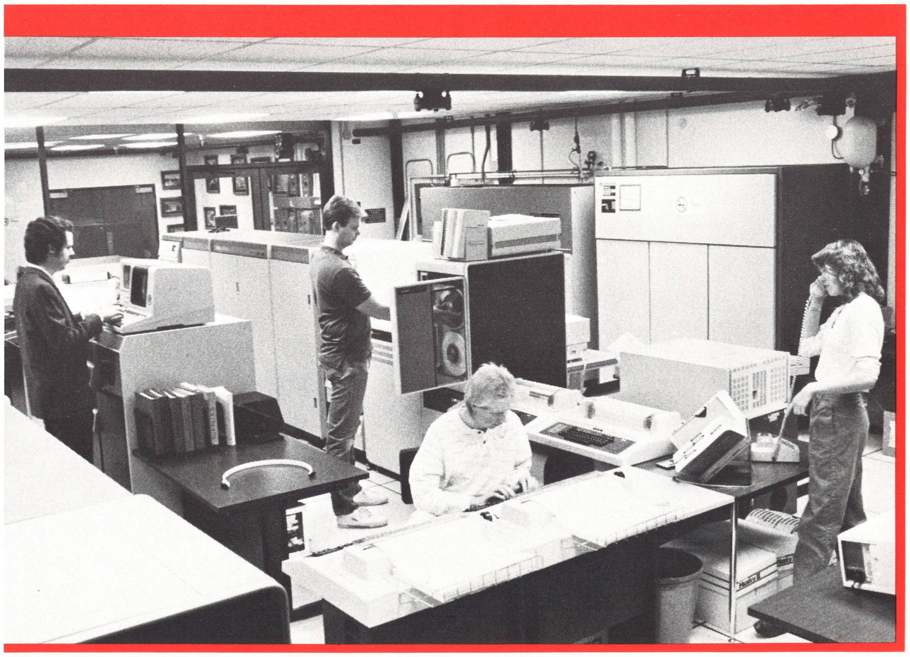
Computer Science Research Computing Facilities

The major research computing facilities in the Department of Computer Science consist of seven laboratories: Software Research Laboratory, Computer Aided Design and Graphics Laboratory, Lisp Programming and Artificial Intelligence Laboratory, Video-Computer Instruction Laboratory, Robotics Laboratory, VLSI Computing Facility and Digital Signal Processing Laboratory. The Software Research Laboratory contains a VAX 8600 used for general purpose timesharing. The Computer Aided Design and Graphics Laboratory contains a DEC VAX 11/785 and special hardware for the display of black and white and color images. The Lisp Programming and Artificial Intelligence Laboratory is the focus for the department's effort in the development of Lisp-based software systems and provides support for several different families of such systems including large Hewlett-Packard 9000 and Apollo Domain networks, as well as a DEC VAX 11/750 for Lisp software development support. The Video-Computer Instruction Laboratory provides an environment of several microprocessor systems and connections to the various host systems used in developing tools for computer aided instruction. The Robotics Laboratory contains several robot arms and special equipment for research in computer vision and image recognition. The VLSI Computing Facility has a dual-processor Gould 9080 and a large number of Apollo and AED color workstations for VLSI design. The Digital Signal Processing Laboratory contains a DEC VAX 11/750 supporting specialized D/A and A/D equipment for real-time signal processing.

The Software Research Laboratory is the primary support facility for research in computer software systems and computer architecture. The DECSystem VAX 8600 provides timesharing services to research projects throughout the department. The DECSystem VAX 8600 currently has 20 megabytes of memory and over four gigabytes of on-line disk storage. The DECSystem 20 is connected to the Arpanet, CSNET and Telenet networks. The VAX 8600 is on the Arpanet and is the local gateway to the USENET and UUCP networks. A BBN Butterfly parallel computer with 18 68020-based processor nodes is in place.

A 10 megabit/second Ethernet provides host-to-host services connecting the DEC System VAX 8600, Graphics Laboratory VAX 11/785, Signal Processing VAX 11/750, Lisp VAX 11/750, VLSI Gould 9080, microvax workstations, Sun workstations and Instructional VAX 11/780. A gateway between the Apollo token ring network and Ethernet is operational, and another gateway to the Hewlett-Packard 9000 network is under development. Gateways effectively give all systems direct access to the Arpanet, USENET, CSNET and UUCP networks. A Sytek LocalNet using broadband coax cable technology provides virtual terminal service to all systems in the department. A large number of laser printers are available throughout the network with distributed laser printers such as the Apple Laserwriter using Postscript becoming the departmental standard. Terminals needing access to multiple machines are connected to specialized terminal interface nodes on the local network instead of hard wired to a particular machine. In order to minimize portability problems, all VAXs and the Gould run under the Unix operating system. The department also makes extensive use of a highly efficient and portable version of Lisp (Portable Standard Lisp) that runs on all host systems and workstations.

Ranked as one of the best in the nation, the department's computing facility offers an outstanding research environment.



The Computer Aided Design and Graphics Laboratory houses a DEC VAX 11/785 as the host computer for many specialized pieces of computer graphics hardware. The VAX has 14 megabytes of main memory and over a gigabyte of disk space. The specialized graphics hardware currently consists of an Evans and Sutherland Multi-Picture System (MPS) and PS 300 for producing high resolution black and white line drawings, a Grinnell 512 x 512 frame buffer and several high resolution color monitors for the production of color pictures and computer generated movies, a Tektronix 4129 color solid modeling system, an Apollo DN660 high resolution color node, and a Lexidata 3D image viewing system. Recent additions include a very high resolution (1536 x 1385 x 24 bits) Chromatics CX1500 color frame buffer and two Silicon Graphics Iris 2400 Systems. This system also drives a Monarch Cortland 45 Direct Numerical Controlled (DNC) machining center.

The Lisp Programming and Artificial Intelligence Laboratory acts as the focus of the department's effort to build a high quality Lisp programming environment on all of the facilities. The laboratory currently has a very large network of Hewlett-Packard 68010 and 68020 based workstations, with approximately 50 nodes in place and with the number expected to double over the next two years. This laboratory also provides Lisp support on the department's Apollo Domain network and timesharing systems, and has a VAX 11/750 to support Lisp software development activities.

The Robotics Laboratory contains Puma and Rhino robot arms, a Vicom real-time image analysis and processing system, and Technical Arts 3D laser range scanner.

The VLSI Computing Facility currently has a dual processor Gould 9080 with 16 megabytes of memory and 2 gigabytes of disk storage. Attached to this facility are 8 AED 512 color workstations for use with numerous VLSI design systems including Magic and Vivid. The laboratory also has a number of stand-alone workstations for VLSI design, including three Apollo 560 color workstations for use with the Mentor system, a Symbolics 3600 and various smaller personal computers.

The Digital Signal Processing Laboratory contains a DEC VAX 11/750 system dedicated to single-user, real-time applications involving image and sound processing. The VAX has 6 megabytes of main memory and several disk drives as well as special analog-to-digital and digital-to-analog hardware and an array processor for real-time use.

Other important departmental facilities include a darkroom and scientific photo laboratory, used in support of the Digital Signal Processing and Computer Aided Design and Graphics Laboratories. The College of Engineering operates a research-scale integrated circuit fabrication facility used heavily by the department. Additionally, the department operates an integrated circuit testing facility used to test and debug both internally and externally fabricated circuits. It contains state-of-the-art Hewlett-Packard, Tektronix and Micromanipulator automated IC testing equipment.

The department also has a DEC VAX 11/780, acquired from and operated with University funds for both undergraduate and graduate instruction. A number of Apollo workstations are used for instruction in computer aided design and digital design courses. The department has many small mini- and microcomputer systems used primarily for instructional purposes and also has obtained a large number of Apple Macintosh computers. The University Computing Center operates a Univac 1100/62 computing system used for service courses taught by the department.

A detailed description of major equipment in the research laboratories follows. Equipment used primarily for instruction is not included.

Significant funding through the NSF/CER program and DARPA, as well as from other private and governmental agencies, have made a major impact on departmental computing resources.

Software Research Laboratory

DEC VAX 8600
  main memory — 20 megabytes
  floating point accelerator
  disk storage — 4 gigabytes
  two nine track tape drives (1600/6250 bpi)
  interface to 10 megabit/second Ethernet
  interface to Arpanet C/30 IMP
  132 asynchronous terminal ports
  PDP 11/34 front-end network communications processor for connection to the TELENET network using X.25
  Hewlett-Packard HP7221S/T four and eight color plotters
3 Sun Microsystems Sun-3 workstations
Arpanet C/30 Interface Message Processor (IMP) and C30 Terminal Access Controller (TAC)
BBN Butterfly Parallel Computer
  18 processing nodes (16 MHz 68020) with floating point (68881)

Digital Signal Processing Laboratory

DEC VAX 11/750
  main memory — 6 megabytes
  floating point accelerator
  disk storage — 1100 megabytes
  nine track magnetic tape drive (800/1600/6250 bpi)
  interface to 10 megabit/second Ethernet
  16 asynchronous terminal ports
  special equipment — DSC 200 dual channel A/D and D/A, FPS Systems 120B floating point processor

VLSI Computing Facility

Gould 9080 dual processor
  main memory — 16 megabytes
  floating point accelerator
  disk storage — 2 gigabytes
  nine track magnetic tape drive (800/1600/ 6250 bpi)
  interface to 10 megabit/second Ethernet
  80 asynchronous terminal ports
  8 AED 512 color VLSI workstations
3 Apollo DN560 color VLSI workstations
Symbolics 3600 Lisp Machine

Computer Aided Design and Graphics Laboratory

DEC VAX 11/785
  main memory — 14 megabytes
  floating point accelerator
  disk storage — 1.3 gigabytes
  Evans and Sutherland Multi-Picture System with one station
  Evans and Sutherland PS 300
  Grinnell GMR27 raster color frame buffer (512 x 512 x 27 bits)
  Lexidata Solidview 3D real-time solid viewing system
  Chromatics CX1500 color frame buffer (1536 x 1385 x 24 bits)
  2 Silicon Graphics IRIS 2400 systems
  Tektronix 4129 color solid modeling system
  Apollo DN660 color workstation
  Barco and Tektronix high resolution color monitors
  Matrix Instruments 9000 series graphics recorder
  Monarch Cortland 45 DNC machining center
  nine track magnetic tape drive (1600/6250 bpi)
  interface to 10 megabit/second Ethernet
  32 asynchronous terminal ports

Robotics Laboratory

Puma 560 robot arm and controller
Rhino robot arm
Technical Arts White scanner 100 3D range scanner
Vicom Image Processing System

Lisp Programming and Artificial Intelligence Laboratory

DEC VAX 11/750
  main memory — 6 megabytes
  floating point accelerator
  disk storage — 550 megabytes
  nine track tape drive (800/1600 bpi)
  interface to 10 megabit/second Ethernet
  32 asynchronous terminal ports
Personal Workstations
  35 HP 9000/300 68020-based Lisp systems, 8 MB each
  10 HP 9000/200 68010-based Lisp systems, 8 MB each
  Hewlett-Packard 2688A laser printer
  Hewlett-Packard SRM network file server
  2 Apollo Domain DN400 system file servers, 160 MB each
  1 Apollo Domain 160 network computer server, 4 MB
  18 Apollo Domain DN300 diskless nodes, 1K x 1K bit mapped displays
  6 Apollo Domain DN330 diskless nodes, 1K x 1K bit mapped displays
  2 Apollo disk server/Ethernet gateway, with 400 MB disk storage
  Apollo GPIB server gateway to VLSI testing system and Text Search system
  2 Sun Mircosystems Sun-2 workstations
  2 VAXstation microvax II workstations

The CAGD group is engaged in research in computer graphics applications, user interfaces, design paradigms, interfaces to manufacturing and analysis, mathematical surface representations and geometric algorithms.

CAD for VLSI Architectures

Principal Faculty

Tony M. Carter
Ganesh C. Gopalakrishnan

Affiliated Faculty

Kent F. Smith

Students and Staff

7 graduate students

Nature of Work

The main objective is to create an object-oriented software and hardware environment to automate as much as possible the process of designing, building and testing systems composed of custom integrated circuits. Using the object-oriented philosophy of system design permits the construction of tools that build upon each other. These tools range from a sophisticated structure editor for integrated circuit design to mixed-mode simulation and automatic test generation.

Current Work Areas

- Production of provably correct designs: Using algebraic specification techniques, circuit designs can be checked for correctness by using formal verification methods such as the Boyer-Moore theorem prover. This approach also provides systematic methods for performing simulation and for the intelligent generation of test vectors.
- Structured techniques for integrated circuit design: Building on past results in the development of Path-Programmable Logic, a new set of design methodologies is being investigated — in particular, a method called "Structured Arithmetic Tiling (or SAT)," which is specially tailored to the implementation of novel arithmetic architectures.
- Design automation: Using structured techniques for circuit design (such as PPL and SAT) as an implementation target, major portions of systems can be designed automatically from correct specifications. System control logic, arithmetic units, register-transfer logic and memory are among the modules currently being studied for automatic generation.
- Object-oriented heterogeneous architectures: A superior environment for the development of systems must have the ability to design computational systems in software and transform them to hardware. Object-oriented systems will be constructed of special-purpose processors, each of which stores particular classes of data objects and performs all operations on the data objects. Communications between classes of objects is via message passing. This architecture has profound implications for the testing and integration of hardware processors in a working environment. Of particular interest is the development of a processor (or set of processors) to aid in the modeling of surface-bounded three-dimensional objects.
- The design of a high-level hierarchical hardware specification language with emphasis on data abstraction, modeling concurrency, specifying structural and behavioral information, and interfacing through translators with VLSI design tools.

Selected Results

Representative publications are:

1. Carter, T. M. "Structured Arithmetic Tiling of Integrated Circuits." Ph.D. Dissertation, University of Utah, Department of Computer Science, 1983.
2. Gopalakrishnan, G. C. "From Algebraic Specifications to Correct VLSI Systems." Ph.D. Dissertation, State University of New York, Department of Computer Science, 1986.
3. Smith, K. F., T. M. Carter, and C. E. Hunt. "Structured Logic Design of Integrated Circuits Using the Stored Logic Array." *IEEE Transactions on Electron Devices* ED-29, no. 4 (Apr. 1982): 765-76.

VLSI researchers inspect the layout of circuit modules used in high-precision, high-speed digital arithmetic units.

4. Carter, T. M., and L. A. Hollaar. "The Implementation of a Radix-16 Digit-Slice Using a Cellular VLSI Technique." *Proceedings of the 1983 IEEE International Conference on Computer Design: VLSI in Computers* (Nov. 1983): 688-91.

Facilities

The CAD for VLSI Laboratory contains three HP 9000/320s, a Symbolics 3600 and access to the Computer Science Department facility having a VAX 8600, VAX 785, VAX 750, and numerous workstations (32 HP 9000/320s, 30 Apollo Domain systems, several microvaxes and several Sun 3s). The laboratory also has access to an integrated circuit test system.

Support

The laboratory is currently supported by a contract from the Defense Advanced Research Projects Agency.

Computer Aided Geometric Design

Principal Faculty

Richard F. Riesenfeld
Elaine Cohen
Spencer W. Thomas

Students and Staff

3 Ph.D. students
5 M.S. students
4 research scientists

Nature of Work

The Computer Aided Geometric Design Group in Computer Science is involved in both fundamental and applied research in developing methods for representations, specifying and manipulating geometric models in a computer. The group is currently engaged in a concerted effort to develop an advanced geometric modeler that is based on mathematical spline representations. Such work involves research in computer graphics applications to the visualization of complex geometric forms, interfaces to analysis packages, interfaces to manufacturing processes, new design paradigms and user interfaces as well as research into new mathematical surface representations and new geometric algorithms. Challenging test cases are provided by sponsoring agencies which help guide this project and keep it in touch with the practical and fundamental issues that concern design as it occurs in industry.

Current Work Areas

- Developing new mathematical forms for representing freeform surfaces.
- Finding new algorithms for operations on spline-based geometric models, including implementing set operations.
- Studying new CAD/CAM architecture.
- Enhancing and extending computer graphics visualization techniques to help the mechanical designer.
- Exploring new modeling pardigms especially suited for computer implementation.
- Defining appropriate interfaces to the manufacturing process.

Selected Results

- For the past three years, the group has been involved in a concerted effort to build an advanced experimental geometric modeler called Alpha_1 which embodies many theoretical and algorithmic advances.

Representative publications are:

1. Cohen, E.; T. Lyche; and R. F. Riesenfeld. "Discrete Box Splines and Refinement Algorithms." *CAGD* (1984).

2. Riesenfeld, R. F. "A View of Spline-based Solid Modeling." *Proc. of Auto-Fact-5* (1983).

3. Cohen, E.; T. Lyche; R. F. Riesenfeld. "An Application of Discrete B-splines to Computer Aided Geometric Design and Computer Graphics." *Computer Graphics and Image Processing* 14, no. 2 (Oct. 1980): 87-111.

4. Cobb, E. S. "Design of Sculptured Surfaces Using the B-spline Representation." Doctoral Dissertation, University of Utah, 1984.

5. Thomas, S. W. "Boolean Operations on Freeform Surfaces." Doctoral Dissertation, University of Utah, 1984.

The scissors model is constructed using Alpha_1, which allows the sophisticated sweeping operation of an arbitrary spline curve.

Facilities

The Computer Aided Design and Graphics Laboratory houses a DEC VAX 11/785 as the host computer for many specialized pieces of computer graphics hardware. The VAX has 12 megabytes of main memory and over a gigabyte of disk space. The specialized graphics hardware currently consists of an Evans and Sutherland Multi-Picture System (MPS) and PS 300 for producing high-resolution black and white line drawings, Grinnell 512 x 512 and Chromatics 1536 x 1152 24-bit frame buffers, and several high-resolution color monitors and a camera station for the production of color pictures and computer generated movies, a Tektronix 4129 color raster system, two Iris 1024 x 768 32-bit workstations, three Sun color raster workstations, and a Lexidata 3D image viewing system. This system also drives a Monarch Cortland 45 Direct Numerical Controlled (DNC) milling machine. The laboratory also has several Apollo color workstations and a Symbolics 3600 Lisp Machine. These systems are used for varied computer aided design activities, with emphasis on integrated circuit design and printed circuit board layout.

Support

The CAGD group is currently supported by grants, contracts and equipment from the National Science Foundation and the U.S. Department of Defense as well as several private sources.

Design and Simulation of Parallel Architectures

Principal Faculty

Richard Fujimoto

Students and Staff

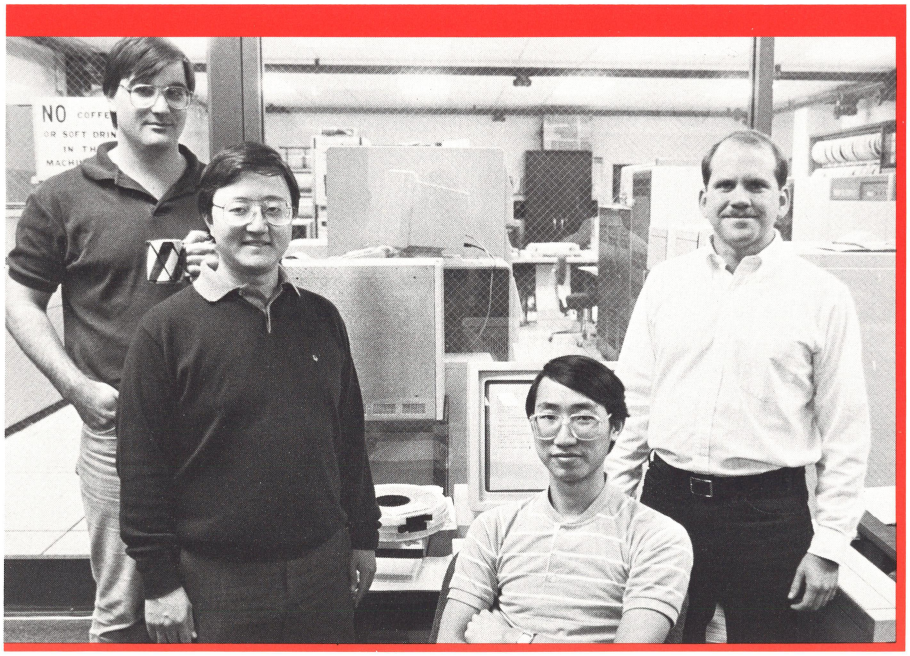
3 Ph.D. students
3 M.S. students

Nature of Work

The parallel computer systems research group is studying the design of high performance multicomputer systems containing hundreds or thousands of powerful microprocessors. Current work is focused on gaining a better understanding of the behavior of the communication network used to interconnect the processors and the development of new techniques to simulate large parallel computers.

Current Work Areas

- Analysis and design of VLSI communication components: This work is oriented to the design and implementation of a general purpose VLSI communication component that can be used to interconnect large numbers of microprocessors in message-based multicomputer systems. Analytic and simulation analyses are used to model the component and evaluate appropriate buffer allocation policies. A VLSI implementation is also under investigation.
- General purpose simulation tools for modeling parallel systems: The Simon project is based on an object oriented, toolkit approach to facilitate rapid development of simulation programs.
- Efficient models of processor behavior and performance: Traditional techniques incur several orders of magnitude overhead to perform instruction level simulation. Such techniques are prohibitively expensive in simulations containing hundreds or thousands of processors. The direct execution method has been developed to improve the efficiency of instruction level simulation by orders of magnitude over previous approaches, often without sacrificing accuracy.
- Distributed simulation: The high computational requirements of discrete event simulation combined with the parallelism inherent in the system being modeled makes simulation a natural candidate for parallel processing. Research in this area focuses on gaining a better understanding of the relationship between parallelism in the system being modeled and speedup when executing the simulation program on a parallel machine. Strategies to map the simulation program on to a parallel architecture are being studied as well as implementation issues.



Utah's simulation and architectures group is studying the design and programming of parallel computer systems.

Selected Results

Representative publications are:

1. Fujimoto, R., and W. Campbell. "Direct Execution Models of Processor Behavior and Performance." Submitted to 1987 Sigmetrics Conference on Measurement and Modeling of Computer Systems.
2. Fujimoto, R. "The Simon Simulation and Development System." *Proc. 1985 Summer Computer Simulation Conference* (July 1985).
3. Fujimoto, R., and S. Swope. "Simon II Kernel Reference Manual." *University of Utah Technical Report No. UUCS-86-001* (March 1986).
4. Fujimoto, R., and S. H. Sequin. "X-Tree and Y-Components." In *VLSI Architecture*, ed. B. Randell and P. C. Treleaven, 299-326, Englewood Cliffs, NJ: Prentice Hall, 1983.
5. Fujimoto, R. "VLSI Communication Components for Multicomputer Networks." Doctoral Dissertation, ERL Report No. UCB/CSD 83/137, University of California, Berkeley, 1983.

Facilities

The principal computing facilities of this project are the Software Research Laboratory DEC VAX 8600 and an 18-node 68020/68881 based multiprocessor called the Butterfly, manufactured by BBN Advanced Computers Inc. Apollo workstations are also used for some of this work.

Principal Faculty

F. Warren Burton

Affiliated Faculty

Ganesh Gopalakrishnan
Gary Lindstrom

Students and Staff

2 Ph.D. students

Nature of Work

The objective of this project is to combine the simplicity of functional programming with the efficiency of procedural programming in the context of distributed computing.

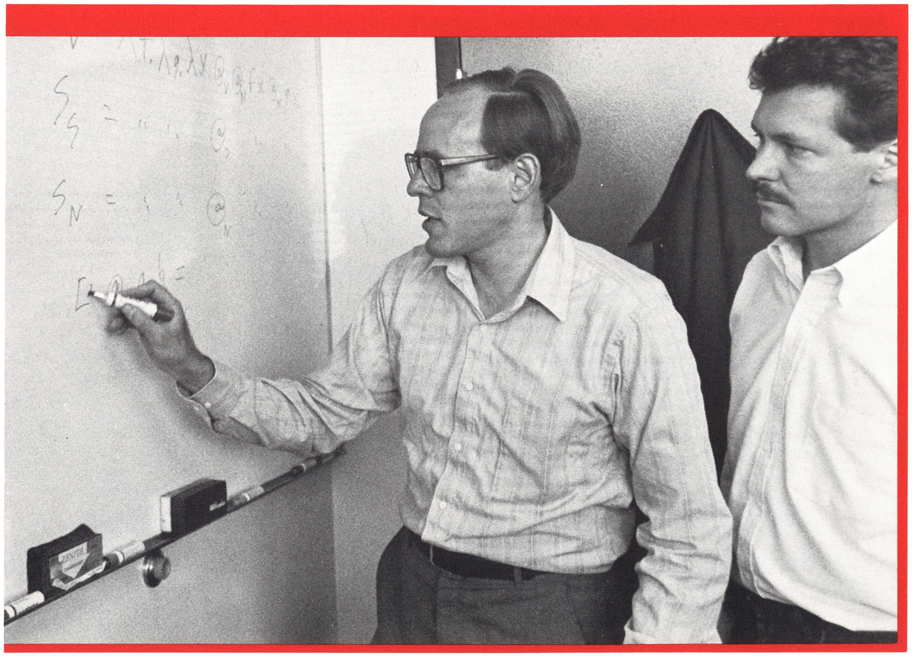
A functional program often is easier than a procedural program to read, write, transform, modify or verify. On the other hand, it is usually easier to control the run-time behavior of a procedural program and, hence, to produce a program that is more efficient than a functional program with respect to time, space and communication requirements. Both ease of use and asymptotic efficiency become increasingly important as parallel and distributed systems are used to solve larger problems.

The researchers' approach is to add annotations to a functional language to control its run-time behavior. The annotations cannot change the result produced by a program (except that a poor choice of annotations can cause nontermination), but may change the way the result is computed.

Related issues such as provisions for nondeterminism, process scheduling and memory management, and applications also are under investigation.

Current Work Areas

- Language design: Control annotations should be added to a functional language in a simple and straightforward manner. Unannotated programs should generally perform in the desired way.
- Speculative computation: Many problems have a low potential for parallelism if no wasted work will be tolerated, but a high potential for parallelism if a system is willing to speculate by performing work that may or may not be required.
- Programming techniques, including the study of abstract data types and higher order functions suitable for functional distributed programming.
- Language implementation: A number of implementation issues are under investigation.
- Scheduling and related issues, including the problem of avoiding memory deadlock for a program known to have reasonable storage requirements when evaluated sequentially.
- Study of applications, including combinatorial search algorithms and graphics algorithms.



Combinators are a useful basis for implementing efficient distributed functional programs.

Selected Results

Representative publications are:

1. Burton, F. W. "Storage Management in Virtual Tree Machines." To appear in *IEEE Trans. Comp.*
2. Burton, F. W.; D. Maurer; H.-G. Oberhauser; and R. Wilhelm. "A Space Efficient Optimization of Call-by-need." To appear in *IEEE Trans. Softw. Eng.*
3. Burton, F. W. "Functional Programming for Concurrent and Distributed Computing." To appear in *Comp. J.*
4. Burton, F. W. "Speculative Computation, Parallelism, and Functional Programming." *IEEE Trans. Comput. C-34*, 12 (Dec. 1985): 1190-3.
5. Joy, M. S.; V. J. Rayward-Smith; and F. W. Burton. "Efficient Combinator Code." *Computer Languages* 10, 3/4 (1985): 212-24.
6. Burton, F. W. "Annotations to Control Parallelism and Reduction Order in the Distributed Evaluation of Functional Programs." *ACM Trans. Program. Lang. Syst. 6*, 2 (Apr. 1984): 159-74.
7. Burton, F. W., and M. M. Huntbach. "Virtual Tree Machines." *IEEE Trans. Comput. C-33*, 3 (Mar. 1984): 278-80.
8. Burton, F. W., and M. M. Huntbach. "Lazy Evaluation of Geometric Objects." *IEEE Comput. Graph. Appl. 4*, 1 (Jan. 1984): 28-33.
9. Burton, F. W. "A Linear Space Translation of Functional Programs to Turner Combinators." *Info. Processing Letters 14*, 5 (23 July 1982): 201-4.

Facilities

This project uses the department's computing facilities, including the VAX 8600, on which several functional languages, including SASL and Miranda, are available. Implementation of a single-processor annotated functional language is in progress, and a simulation to determine its performance on a distributed computer system is planned.

Support

This project has received support from the National Science Foundation, NATO and the Amoco Production Company.

Information-based Complexity

Principal Faculty

Krzysztof A. Sikorski

Affiliated Faculty

Terry Boult, Columbia University
Henryk Wozniakowski, Columbia University
Frank Stenger

Nature of Work

The research in information-based complexity involves the design of optimal algorithms (i.e., algorithms having minimal cost) for solving problems for which only partial, priced or contaminated information is available. Such problems arise in many disciplines including economics, computer science, medicine, scientific and engineering computation, geophysics and others.

Current Work Areas

- Complexity of solving nonlinear equations: Optimal or nearly optimal algorithms are investigated for various error criteria and classes of functions.
- Complexity of the topological degree (jointly with Terry Boult): Nearly optimal algorithms are designed for exact computation of Topological Degree of Lipschitz functions in arbitrary number of dimensions.
- Complexity of fixed points (jointly with Henryk Wozniakowski): Optimal algorithms are designed for approximation of fixed points of contractive mappings.
- Nonlinear integral and differential equations (jointly with Frank Stenger): Nearly optimal algorithms are investigated for the approximate solution of these problems.
- Complexity of linear programming: New algorithms are being developed to improve available complexity bounds.

Information-based complexity develops smallest-cost algorithms for approximately solved problems.

Selected Results

Most of the current results are summarized in the review paper (1) and papers (2, 3, 4). They involve optimal algorithms for zero finding problems in classes of smooth functions, functions with non-zero topological degree and functions satisfying a Lipschitz condition.

Representative publications are:

1. Sikorski, K. "Optimal Solution of Nonlinear Equations." *Journal of Complexity* 1, no. 2 (1985): 197-209.
2. Boult, T., and Sikorski, K. "Complexity of Computing Topological Degree of Lipschitz Functions in N-Dimensions." *Journal of Complexity* 2 (1986): 46-59.
3. Sikorski, K., and H. Wozniakowski. "For Which Error Criteria Can We Solve Nonlinear Equations?" *Journal of Complexity* 2 (1986): 163-78.
4. Sikorski, K. "Bisection is Optimal." *Numerische Mathematik* 40 (1982): 111-17.
5. Sikorski, K., and F. Stenger. "Optimal Quadratures in Hp Spaces." *ACM Transactions on Mathematical Software* 10 (1984): 140-51.

Facilities

This project uses general department facilities such as DEC 2060 and VAX 8600.

Support

This project is currently supported by an AMOCO engineering grant and was supported in the past by National Science Foundation and Defense Advanced Research Projects Agency contracts.

Information Retrieval and Manipulation

Principal Faculty

Lee A. Hollaar

Students and Staff

3 Ph.D. students
2 M.S. students
3 staff programmers

Nature of Work

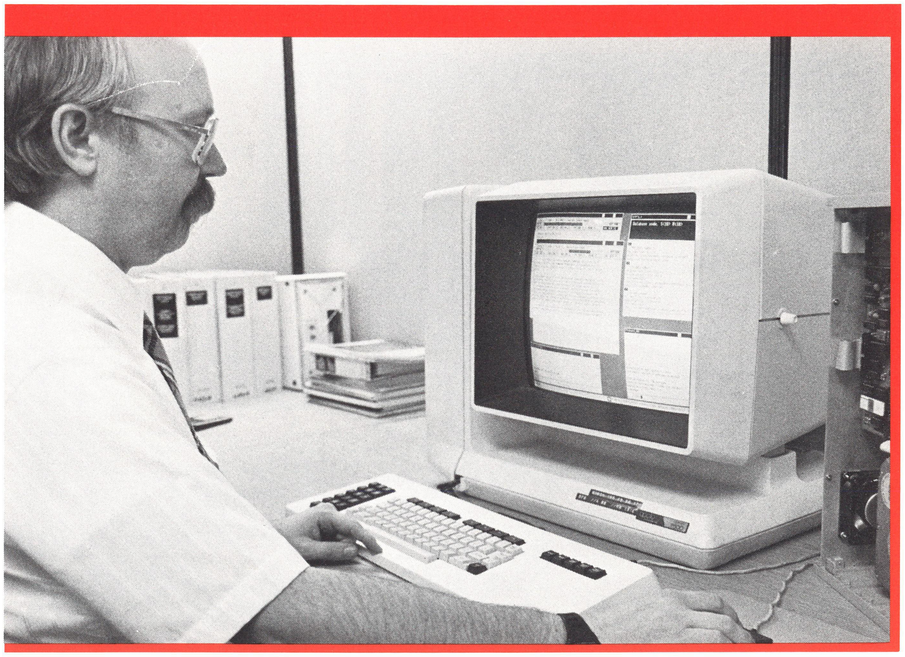
The Utah Retrieval System Architecture (URSA) project is developing well-engineered solutions to the implementation of very large (50 billion characters or more), rapid (average response time of ten seconds) text information retrieval and manipulation systems. The project has three major components. Perhaps the best known is the work on specialized backend processors, particularly high-speed search engines, capable of replacing software modules and dramatically improving overall system performance. The other two project components are the development of distributable computer applications and improvements to the user interface for information retrieval systems.

The internal structure of the URSA system is based on a high-level data communications protocol dynamically linking client modules (such as the user interface) to servers (such as index processors and search engines). This allows the modules to be easily distributed in a multi- or specialized-processor configuration as well as allowing the system to run on a single processor. It also allows new modules, or functional replacements for existing system modules, to be added to the system while it is in operation.

The work on the user interface concentrates not only on the syntax and semantics of the query language, but also on the overall user environment. Enhancements over conventional information retrieval systems include convenient ways to browse through retrieved documents, access to other information retrieval systems through gateways supporting a common command interface, and interfaces to word processing and other specialized functions.

Current Work Areas

- Improvements to the prototype search engine, implemented using custom VLSI circuits.
- Enhancements to the existing demonstration text retrieval system.
- Measurement and evaluation of the architecture running in a variety of configurations.
- Improvements to the fault tolerance and system security provided by the distributable architecture.



The Utah retrieval system architectures project has implemented a prototype distributed information retrieval system. Shown is the window-based user interface running on an Apollo workstation, and a high-speed search engine implemented using custom VLSI circuits.

Selected Results

Representative publications are:

1. Hollaar, L.; K. Smith; W. H. Chow; R. Haskin; and P. Emrath. "The Architecture and Operation of a Large, Full-text Information Retrieval System." International Workshop on Database Machines (August 1982); also *Advanced Database Machine Architecture*, Chapter 9, Prentice-Hall, 1983.
2. Hollaar, L., and R. Haskin. "Operational Characteristics of a Hardware Pattern Matcher." *ACM Transactions on Database Systems* (March 1983).
3. Hollaar, L. "A Testbed for Information Retrieval Research: The Utah Retrieval System Architecture." Eighth Annual International ACM SIGIR Conference, Montreal, June 1985.
4. Hollaar, L. "A Workstation-based Approach to Text Retrieval and Manipulation." First International Conference on Computer Workstations, San Jose, November 1985.
5. Zeleznik, M. "A Portable, Network-transparent Communication System for Message-based Applications." Sixth International Conference on Distributed Computing Systems, Cambridge, MA, May 1986.

Facilities

The project is a major user of the departmental computer facilities. The demonstration text retrieval system is being implemented on the Apollo Domain workstation network. The project also has a number of IBM Personal Computers and a Compaq. The development of the text search processor custom VLSI circuit is being done using the ComputerVision system, with prototype fabrication in the College of Engineering's HEDCO Microelectronics Laboratory.

Support

The development of the text search engine has been supported by the National Science Foundation. Development of the information retrieval system has been supported by NSF and other government agencies as well as Digital Equipment Corporation. The design of the VLSI design database system was supported by the NSF and International Business Machines.

Principal Faculty

Richard C. Brandt

Students and Staff

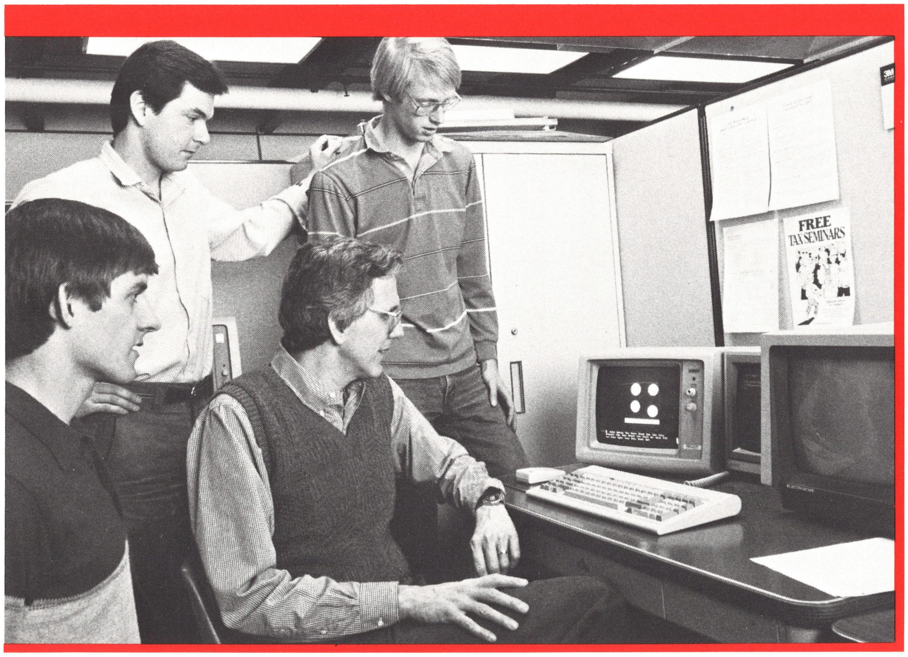
Bradley N. Davis
1 M.S. student
3 additional graduate and undergraduate students

Nature of Work

The group has developed tools for the implementation of knowledge-based instruction on microcomputers and minicomputers. The tools range from compilers to create databases for knowledge-based games (the Computer-based Memorization System) to editors for creating knowledge-based micro-worlds (the Equipment Problem Solving System). Current work is concentrated on refining these tools and the development of student models. The knowledge is represented primarily in semantic networks and production rules.

Current Work Areas

- Refinement of the authoring and implementation tools for the UNIX and MS-DOS environments.
- Development of tools to create student models.
- Development of instructional management tools.



The instructional software systems group develops authoring tools for knowledge-based computer-aided design (CAI).

Selected Results

1. Brandt, R.C. "Equipment Problem Solving Techniques — Author's Manual." University of Utah, 1986.

Support

The majority of the work has been supported by the Navy Personnel Research and Development Center.

Parallel Programming

Principal Faculty

Gary Lindstrom

Affiliated Faculty

Warren Burton
Ganesh C. Gopalakrishnan
Robert R. Kessler

Students and Staff

3 Ph.D. students
3 M.S. students
1 programmer

Nature of Work

The Parallel Programming Research Group seeks to construct high-quality programming systems suitable for the general-purpose exploitation of multiprocessor computer architectures. This effort addresses:

- Design of nontraditional programming languages,
- Implementation of these languages on multi- and single-processor systems, and
- Demonstration of their effectiveness for sound software engineering on significant problems.

Current Work Areas

- The design and implementation of multi-paradigm languages, based on selective combinations of functional, logic, object-oriented and constraint-based concepts.
- Investigation of graph reduction as a strategy for representing and distributing program execution. Originally conceived as an architectural framework for normal order functional languages, graph reduction is now being extended to support other paradigms, notably logic programming.
- Development of efficient techniques for compiling graph reduction to native code for conventional multiprocessors. Using strictness analysis, this provides an attractive mechanism for interfacing functional programming to both imperative (e.g., object-oriented) code and optimized logic programs (e.g., compiled to Warren Abstract Machine code).
- Construction of new algorithms that exploit the advantages of parallel programming: Of particular interest are problems having determinate overall results, despite the use of indeterminate intermediate values.
- Examination of software engineering issues in parallel programming, including programming environments, debugging and performance evaluation.

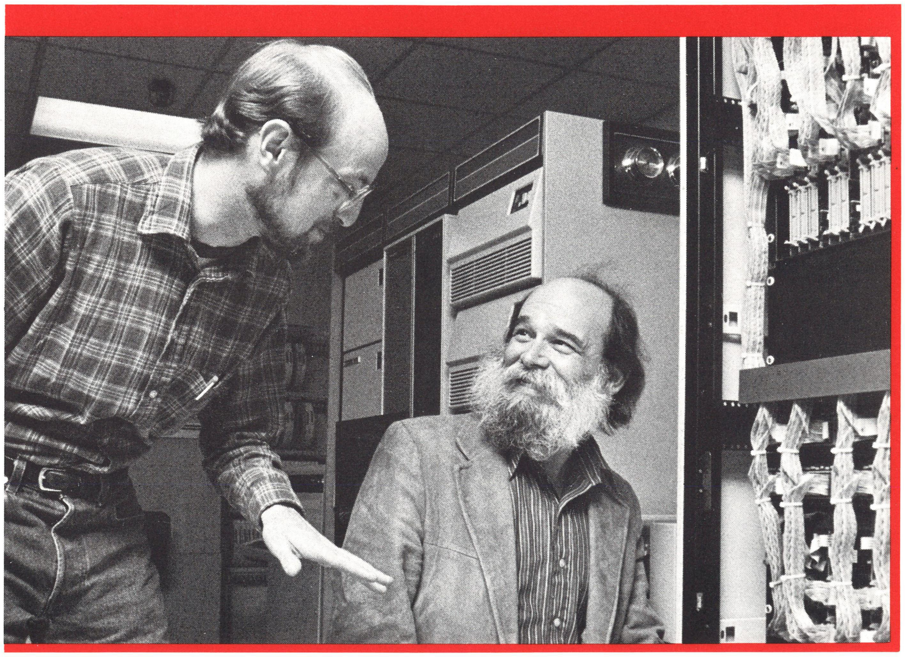
Selected Results

Representative publications are:

1. Lindstrom, G., and P. Panangaden. "Stream-based Execution of Logic Programs." In *Proc. Int'l. Symp. on Logic Programming Conf.,* 168-76. IEEE Computer Society, Atlantic City, NJ, Feb. 1984.

2. Lindstrom, G. "OR-Parallelism on Applicative Architectures." In *Proc. 2nd Int'l. Logic Programming Conf.,* 159-70. Uppsala University, July 1984.

3. Lindstrom, G. "Functional Programming and the Logical Variable." In *Proc.*



The parallel programming research group makes extensive use of its BBN Butterfly multiprocessor system.

Symp. on Princ. of Programming Lang., 266-80. ACM, New Orleans, Jan. 1985.

4. Lindstrom, G. "Static Evaluation of Functional Programs." In *Proc. Symposium on Compiler Construction,* 196-206. ACM SIGPLAN, Palo Alto, CA, June 1986.
5. Lindstrom, G. "Implementing Logical Variables on a Graph Reducation Architecture." In *Proc. Santa Fe Workshop on Graph Reduction,* ed. R.M. Keller and J. Fasel. Springer-Verlag, 1987.
6. Lindstrom, G.; L. George; and D. Yeh. "Generating Efficient Code from Strictness Annotations." In *Proc. TAPSOFT 87, Joint Conference on Theory and Practice of Software Development.* University of Pisa, Italy, March 1987.

Facilities

The principal computing facility of the project is an 18-node 68020/68881 Butterfly Parallel Processor, manufactured by BBN Advanced Computers Inc. Extensive use is also made of Hewlett-Packard 9000/320 workstations as well as the Software Research Laboratory DEC VAX 8600, which serves as the Butterfly host.

Support

The project has received support from the National Science Foundation, Hewlett-Packard Corporation, International Business Machines Corporation, Microelectronics and Computer Technology Corporation and L. M. Ericsson Telefon AB.

Principal Faculty

Robert R. Kessler

Students and Staff

6 graduate students
2 undergraduate students
2 senior systems programmers

Nature of Work

The UTAH Portable AI Support System (PASS) project is developing portable systems capable of supporting AI research and other diverse symbolic computation applications such as algebra, CAGD and VLSI. The portable compiler is the root of portable systems, and research is directed toward showing that a highly optimizing compiler will produce a more productive environment. The key to the system's portability is the incorporation of an architectural description language into all phases of the compiler. This compiler is then used as a "systems programming language" to implement a uniform environment across many different machines; this has been realized in the Utah Portable Standard Lisp (PSL) project in which PSL runs on architectures ranging from the Motorola 68000s to the CRAY X/MP. The PASS compiler has been initially implemented for PSL, although there are plans to implement other systems, such as Common Lisp and PROLOG, using PSL as the implementation language (much as C might be the implementation language).

Emphasizing Lisp as the implementation language provides a language that not only operates efficiently in the symbolic world, but also adapts well to "number crunching." PSL will be extended to support datatype analysis at compile time, emphasizing efficient floating point computation to aid applications like the Utah CAGD, robotics and VLSI projects.

Current Work Areas

- Architectural description-driven compilation.
- Object-oriented programming styles and techniques within Lisp.
- Compiler writing systems.
- Software portability.
- Lisp for multiprocessors.
- Lisp system implementation.
- Innovative symbol manipulation methods (hashing, pattern matching, etc.)
- Expert systems for program analysis and rule-based compilation.

Selected Results

The Experimental Portable Standard Lisp Compiler (EPIC) is a compiler testbed for experimentation with, and development of, Lisp compilation strategies. The goal of the project is to develop a highly optimizing, highly portable Lisp compiler. EPIC performs three main forms of optimizations: source-to-source transformations, register allocation and peephole optimization. The central feature of EPIC is its register allocator. Most other Lisp compilers compile code which

The Lisp programming laboratory has been a major beneficiary of a $5 million Hewlett-Packard artificial intelligence workstation equipment gift.

passes parameters in the stack. PSL and PCLS expect arguments in machine registers, thus making register allocation of crucial importance in the Utah systems. The portability is based on an "architectural description" of the target machine.

MicroScope is an AI-based system for analyzing Lisp programs as well as a collection of tools for analysis and debugging of software systems written in Lisp. The tools are tied together with a common data representation and a common Prolog rule system. The Prolog system is written in Lisp and is optimized for dealing with MicroScope data objects. The components of MicroScope include: static analysis, execution monitoring, post-mortem analysis, and plan extraction and analysis.

The Portable Common Lisp Subset (PCLS) is a first attempt at allowing experimentation with some of the issues involved in the implementation of Common Lisp. It is a PSL program that implements an 80% subset of Common Lisp. It performs default lexical scoping but does not provide support for closures. The other main parts omitted from the system are a few data types (complex numbers, rational numbers, stream, etc.) and their associated functions. The implementation of PCLS has provided the PSL user community (now over 500 sites worldwide) with the opportunity to join the mainstream of Lisp development with Common Lisp.

In a joint research project with Schlumberger Palo Alto Research Labs, the PASS project is investigating language design, compilation and resource allocation for the FAIM-1 Symbolic Multiprocessing System. Researchers are designing a Lisp-based, object-oriented language (based on Scheme) to be used as both the systems and applications language for FAIM. Programs will be written in this language as a collection of fine- and medium-grained objects communicating with each other via messages. Being developed is a compiler and resource allocator to effectively utilize the resources of the FAIM-1 architecture.

The FROBS research project is developing a system that combines, into one system, the features of frames and objects as a data and knowledge representation tool. An important goal of this project is the creation of a uniform data structure allowing the user to develop either regular Lisp code or rule-based code to manipulate the data. There is no need to convert between the two representations, as they are one and the same. Some of the other goals of this project are to have the ability to attach daemons to the objects, to have context-based multiple inheritance and to have methods act like functions.

Representative publications are:

1. Kessler, R.; J. Peterson; H. Carr; G. Duggan; J. Knell; and J. Krohnfeldt. "EPIC — A Retargettable, Highly Optimizing Lisp Compiler." *Proceedings of the SIGPLAN '86: Symposium on Compiler Construction* (June 1986): 118-30.

2. Kessler, R.; S. Shebs; W. Galway; and S. Loosemore. "A Portable Common Lisp Subset with High Performance." *Utah PASS Opnote* 86-01 (February 1986).

3. Krohnfeldt, J., and R. Kessler. "MicroScope — Rule-based Analysis of Programming Environments." *Proceedings of the 2nd Conference on Artificial Intelligence Applications." IEEE* (December 1985).

4. Carr, H., and R. Kessler. "A Forth-based Object File Format and Relocating Loader Used to Bootstrap Portable Standard Lisp." *The Journal of Forth Application and Research* 3-2 (1985): 119-22.

5. Kessler, R. "Peep — An Architectural Description Driven Peephole Optimizer." *SIGPLAN '84: Symposium on Compiler Construction* (June 1984).

Facilities

The main computing activity of the group is centered on the group's Hewlett-Packard 9000 series AI workstations with central facilities provided by the group's VAX 750.

Support

The research activities of the group have been funded by several agencies and many industrial sponsors.

University of Utah

Department of Computer Science
3190 Merrill Engineering Building
Salt Lake City, Utah 84112
(801) 581-8224

Cover photographs:
(Computer) Jedrzej
Borowczyk, (Skiing) Salt
Lake Valley Convention and
Visitors Bureau and
(Campus) John Telford,
Instructional Media
Services.

VLSI Design Methodologies

Principal Faculty

Kent F. Smith

Affiliated Faculty

Tony M. Carter
Ganesh C. Gopalakrishnan

Students and Staff

4 graduate students
1 programmer

Nature of Work

The primary focus of this research is on the development of structured techniques for integrated circuit design, especially Path-Programmable Logic (PPL) and memory generation. This research effort is closely allied with the CAD for VLSI program. Of primary interest is the application of structured design techniques of new implementation technologies.

Current Work Areas

- Automatic test generation for PPL circuits: By examining the row and column structure of PPL circuits, intelligent choices about testing are made to minimize test time while maintaining reasonable fault coverage.
- Implementation of PPL in the CMOS and GaAs implementation technologies: GaAs imposes special restrictions on circuit design that can be easily and automatically enforced through the use of PPL.
- Automatic generation of static memory modules: Given a desired memory aspect ratio (word width and address space), memory modules are completely generated including storage, sense amplifiers and interface to CMOS PPL.
- Alpha_1 processor components: As part of the Alpha_1 surface processor architecture, integrated circuits are being designed using PPL and related methods that will greatly enhance the performance of surface operations.

Selected Results

Representative publications are:

1. Smith, K. F.; T. M. Carter; and C. E. Hunt. "Structured Logic Design of Integrated Circuits Using the Stored Logic Array." *IEEE Transactions on Electron Devices* ED-29, no. 4 (April 1982): 765-76.

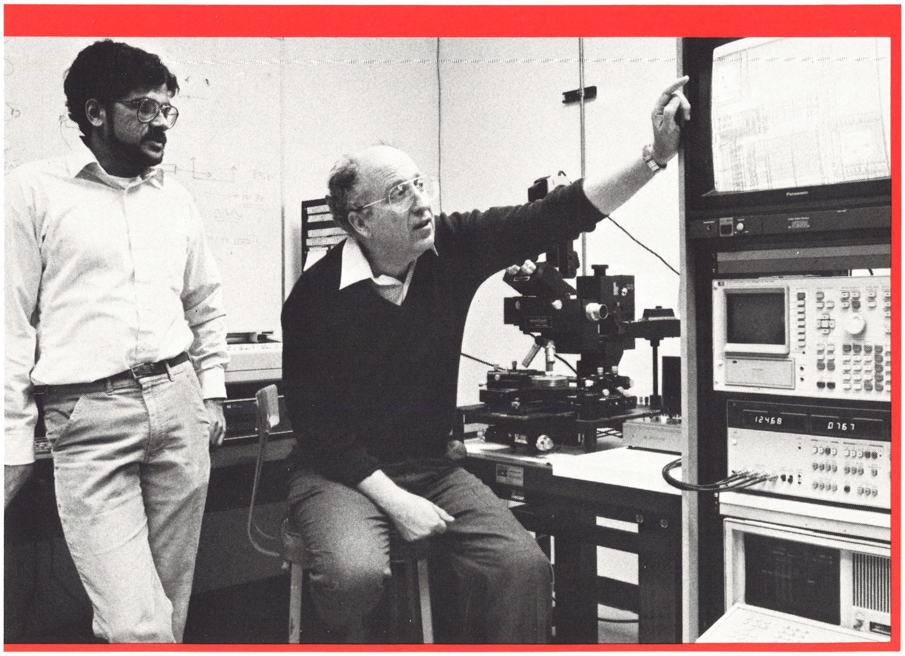
2. Israelson, P. D., and K. F. Smith. "Comparison of the Path-Programmable Logic Design Methodology with Other Custom and Semicustom Approaches." *Proceedings of the 1985 IEEE International Conference on Computer Design: VLSI in Computers* (Oct. 1985): 73-6.

Facilities

The VLSI Design Laboratory makes extensive use of three Apollo DN 560s, integrated circuit test equipment and the College of Engineering Gould 9080 computer. Also available is the Computer Science Department facility having a Symbolics 3600, VAX 8600, VAX 785, VAX 750 and numerous workstations (35 HP 9000/320s, 30 Apollo Domain systems, several microvaxes and several Sun 3s).

Support

The VLSI design project is currently supported through contracts with the Defense Advanced Research Projects Agency and the National Science Foundation.



VLSI researchers test a fabricated circuit to verify correct function and measure performance.

Principal Faculty

Bir Bhanu
Thomas C. Henderson

Students and Staff

10 graduate students
2 undergraduate students

Nature of Work

The research program is directed toward solving both practical and theoretical problems in robotics, vision and sensory control. The design and development of complete robotic systems are of central concern as are individual components of such systems. In particular, the group is studying high-level control of a multifingered robot hand, contact sensors for the hand, image processing and pattern recognition aspects of the robot hand, multisensor integration systems, 3D sensing systems, representations and modeling of objects, computation of salient grasping and manipulation features, and industrial tasks.

A major area of work is computer aided geometric design (CAGD)-based computer vision for recognition and manipulation of 3D objects. Work also is progressing on the segmentation, classification and contextual cueing algorithms, and on the evaluation of various image processing and pattern recognition algorithms and expert systems.

Current Work Areas

- CAGD-based vision analysis.
- Low-level representations of sensor data.
- Logical sensor specification and multisensor integration.
- Representation and models of 2D and 3D objects.
- Multisensor knowledge systems.
- Evaluation of pattern recognition and image analysis algorithms.
- Contextual cueing, expert systems.
- Multifingered hand control using vision and tactile sensors.
- Robot hand grasping and manipulation strategies.
- Robot-task specifications.

Selected Results

Representative publications are:

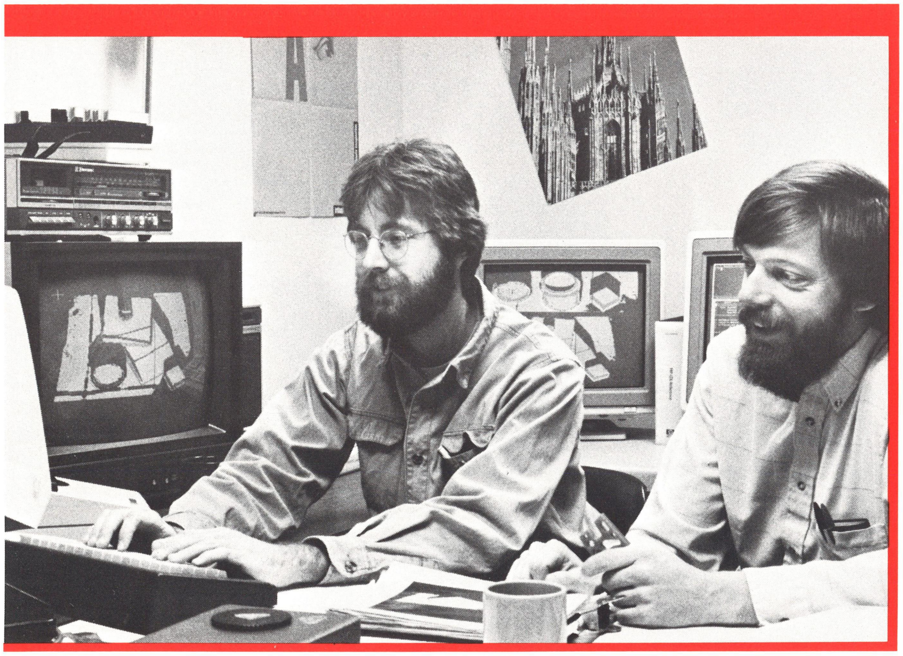
1. Bhanu, B. "Representation and Shape Matching of 3D Objects." IEEE Transactions on Pattern Analysis and Machine Intelligence, *PAMI-6* (May 1984): 340-51.
2. Bhanu, B., and O. D. Faugeras, "Shape Matching of Two-dimensional Objects." IEEE Transactions on Pattern Analysis and Machine Intelligence, *PAMI-6*, (March 1984): 137-56.
3. Bhanu, B., and O. D. Faugeras. "Segmentation of Images Having Unimodel Distributions." IEEE Transactions on Pattern Analysis and Machine Intelligence, *PAMI-4* (July 1982): 408-19
4. Bhanu, B., and J. H. McClellan. "On the Computation of Complex Cepstrumm." IEEE Transactions on Acoustics, Speech, and Signal Processing, *ASSP-38* (Oct. 1980): 583-5.
5. Henderson, T. C., and E. Shilcrat. "Logical Sensor Specification." *Journal of Robotic Systems* 1, no. 2 (1984): 169-93.
6. Henderson, T. C., and W. S. Fai. "MKS: A Multisensor Kernel System." *IEEE Transactions on Systems, Man and Cybernetics* SMC-14, no. 5 (Sept./Oct. 1984): 784-91.
7. Henderson, T. C. "Efficient 3D Object Representations for Industrial Vision Systems." Special issue of *IEEE Transactions on Pattern Analysis and Machine Intelligence* (Nov. 1983): 609-18.
8. Mohr, R., and T. C. Henderson. "Arc and Path Consistency Revisited." *Artificial Intelligence* 28, no. 2 (March 1986): 225-33.

Facilities

In addition to a VAX 11/750 and graphics facilities, the computer vision and robotics group has a Rhino XR-1 six-degree-of-freedom robot arm, a Unimate PUMA 560 six-degree-of-freedom arm, a VICOM Image Processor and a laser range-finder White scanner. The graphics facilities provide a suitable environment for simulations, and the Mechanical Engineering Department's Center for Engineering Design complements the research of the robotics group by allowing first-hand experience with the latest in robotics technology such as the multifingered hand.

Support

Computer vision and robotics research is supported by grants from the National Science Foundation and the Army Research Office.



The computer vision and robotics research program is directed toward solving problems in robotics vision and sensory control.

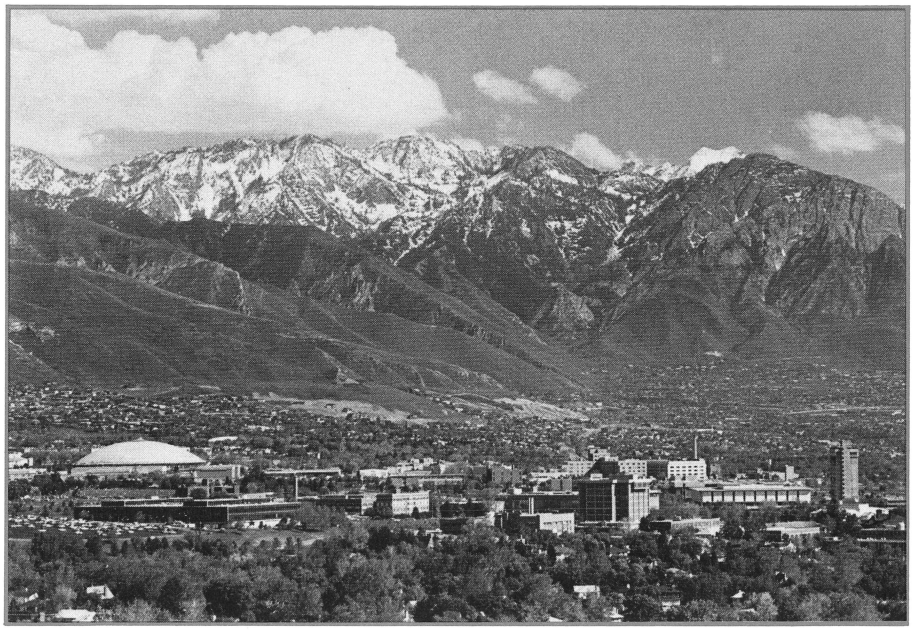
Focus on Current Research
Computer Science
at the University of Utah

Contents

Faculty 2
Research Computing Facilities 3

Current Research Projects

  Applicative Multiprocessing Systems 5
  Computer Aided Geometric Design 6
  Computer Music 7
  Object-based Architectures 8
  Portable AI Support System 10
  Robotics and Computer Vision 11
  Text Retrieval 13
  Video-computer Courseware Implementation System 14
  Very Large Scale Integration 15



More than half of the University's permanent buildings have been constructed since 1960. The 1,500-acre campus is nestled at the base of the Wasatch Mountains and overlooks downtown Salt Lake City.

Faculty

Chairman
Richard F. Riesenfeld, Ph.D.

Professors
Robert E. Barnhill, Ph.D.
Robert M. Keller, Ph.D.
Elliott I. Organick, Ph.D.
Richard F. Riesenfeld, Ph.D.
William J. Viavant, Ph.D.

Associate Professors
Thomas C. Henderson, Ph.D.
Lee A. Hollaar, Ph.D.
Gary E. Lindstrom, Ph.D.
Kent F. Smith, Ph.D.

Assistant Professors
Bir Bhanu, Ph.D.
Tony M. Carter, Ph.D.
Richard Fujimoto, Ph.D.
P. A. Subrahmanyam, Ph.D.
Spencer Thomas, Ph.D.

Research Associate Professors
Richard Brandt, Ph.D.
Elaine Cohen, Ph.D.
Ercolino Ferretti, B.M.

Research Assistant Professors
Brent S. Baxter, Ph.D.
Robert Kessler, Ph.D.
Lewis C. Knapp, Ph.D.

Adjunct Professors
David C. Evans, Ph.D.
Thomas G. Stockham Jr., Sc.D.

Adjunct Associate Professor
David Hanscom, Ph.D.

Instructor
William Salmon, Ph.D.

Computer science research and instruction are centered in Merrill Engineering Building, a 440,000-square-foot facility housing the seven departments of the College of Engineering.

Computer Science Research Computing Facilities

Six laboratories comprise the major research computing facilities in the Department of Computer Science: Software Research Laboratory, Computer Aided Design and Graphics Laboratory, Small Computer Laboratory, Video-computer Instruction Laboratory, Robotics Laboratory and Digital Signal Processing Laboratory.

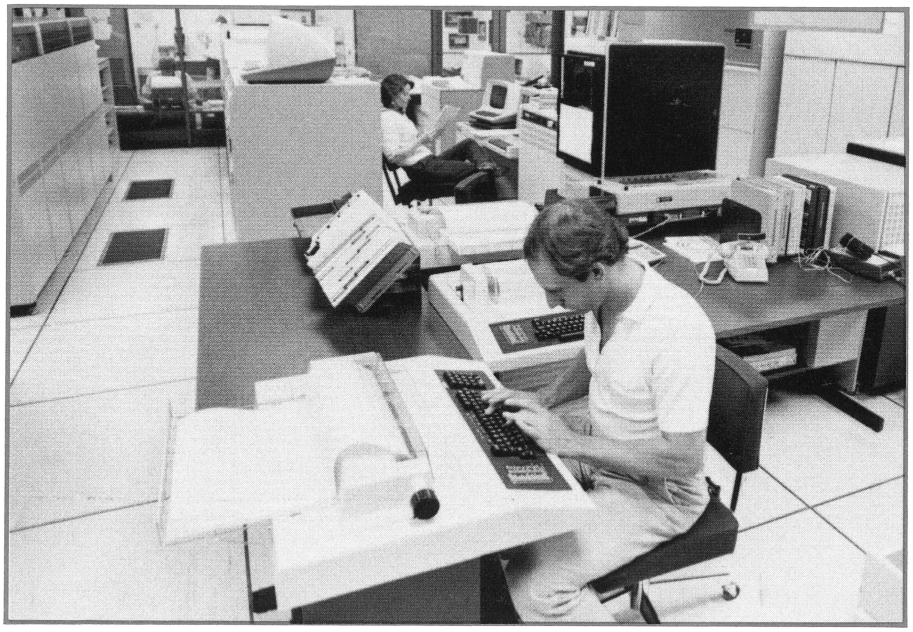
The Software Research Laboratory contains a DECSystem 2060 computer and a VAX 11/750 which are used for general-purpose timesharing. The Computer Aided Design and Graphics Laboratory has a DEC VAX 11/750 and special hardware for the display of black and white and color images as well as a dedicated ComputerVision system for integrated circuit design and a Symbolics 3600 LISP Machine.

The Small Computer Laboratory is the focus of the department's development of a professional workstation environment. It also provides support for several different families of systems including a large Apollo Domain and Hewlett-Packard 9836 networks, and various other 16- and 32-bit microprocessor systems as well as a DEC VAX 11/750 for LISP software development support.

The Video-computer Instruction Laboratory provides several microprocessor systems and connections to various host systems used in developing tools for computer aided instruction. The Robotics Laboratory contains several robot arms and special equipment for research in computer vision and image recognition. The Digital Signal Processing Laboratory contains a DEC VAX 11/750 supporting D/A and A/D equipment for real-time signal processing.

The Software Research Laboratory is the primary support facility for research in computer software systems and computer architecture. The DECSystem 2060 provides timesharing services to research projects throughout the department. The DECSystem 2060 currently has over five megabytes of memory and more than a gigabyte of on-line disk storage. The system has the usual complement of peripherals such as tape drives and printers as well as several special output devices including four- and eight-color plotters, a Mergenthaler Omnitech/2000 on-line digital photocomposer, and Xerox 2700 and DEC LN01 laser printers. The DECSystem 20 is connected to three networks: ArpaNet, CSNet and Telenet. A DEC VAX 11/750 provides additional computing power and program development support for several real-time systems including the Graphics Laboratory and Digital Signal Processing Laboratory. The VAX 11/750 is also on the ArpaNet and is the local gateway to USENET and UUCP.

A ten megabit/second Ethernet provides host-to-host services connecting the DECSystem 20, VAX 11/750, Graphics Laboratory VAX 11/750, Signal Processing VAX 11/750, Small Computer Laboratory VAX 11/750, Sun workstations, and Instructional VAX 11/780. There is a gateway between the Apollo token ring network and Ethernet, and another gateway to the Hewlett-Packard 9836 network is being developed. Gateways effectively give all systems direct access to the ArpaNet, USENET, CSNet and UUCP networks. A Sytek LocalNet using broadband coax cable technology provides virtual terminal service to all systems in the department. Terminals that need access to multiple machines are connected to specialized terminal interface nodes on the local network instead of being hard-



The central research computing facility provides general purpose timesharing resources for research projects throughout the department.

wired to a particular machine. In order to minimize portability problems, all VAXs run under the UNIX operating system. There is a UNIX-compatible compiler and environment for the C programming language on the DECSystem 20. The department also makes extensive use of an efficient portable version of LISP (Portable Standard LISP) that runs on all host systems and workstations.

The Computer Aided Design and Graphics Laboratory houses a DEC VAX 11/750 as the host computer for many specialized pieces of computer graphics hardware. The VAX has six megabytes of main memory and over a gigabyte of disk space. The specialized graphics hardware currently consists of an Evans and Sutherland Multi-Picture System (MPS) and PS 300 for producing high-resolution black and white line drawings, a Grinnell 512 x 512 frame buffer and several high-resolution color monitors for the production of color pictures and computer generated movies, a Megatek 7290 color raster line-drawing system, and a Lexidata 3D image viewing system. This system also drives a Monarch Cortland 45 Direct Numerical Controlled (DNC) milling machine. Several acquisitions — including a very high-resolution (1280 x 1024 x 32 bit) color frame buffer — are in progress. The laboratory also has a ComputerVision Designer CAD system with two interactive design stations and a Symbolics 3600 LISP Machine. These systems are used for varied computer aided design activities, with emphasis on integrated circuit design and printed circuit board layout. Attached to this system is a very high-speed Calcomp 960 plotter for hard-copy output.

The Small Computer Laboratory acts as the focus of ongoing activities in the development of an environment supporting professional bit-mapped workstations, which are being installed throughout the department. This laboratory contains the central support nodes and file servers for the department's Apollo Domain network and gateway to the host-based Ethernet. Equipment also includes a large network of Hewlett-Packard 9836 workstations that are used primarily for LISP (PSL) development.

The Robotics Laboratory contains both Puma and Rhino robot arms and special equipment for digital image recognition and computer vision.

The Digital Signal Processing Laboratory contains a DEC VAX 11/750 system dedicated to single-user, real-time applications involving image and sound processing. The VAX has three megabytes of main memory and several disk drives as well as an array processor and special analog-to-digital and digital-to-analog hardware.

Other important departmental facilities include a darkroom and scientific photo laboratory used to support the Digital Signal Processing and Computer Aided Design and Graphics laboratories. The College of Engineering operates a research-scale integrated circuit fabrication facility which is used heavily by the department. Additionally, the department has an integrated circuit testing facility containing state-of-the-art Hewlett-Packard, Tektronix and Micromanipulator automated IC testing equipment used to test and debug internally and externally fabricated circuits.

The department's DEC VAX 11/780 was acquired and is funded by the University for undergraduate and graduate instruction. Numerous mini and microcomputer systems are used primarily for instruction, and a large number of Apple Macintosh computers are being purchased. The University Computer Center operates a Univac 1100/61 computing system which is used for service courses taught by the department.

A wide array of advanced computer graphics equipment is used by projects ranging from computer aided design to robotics and VLSI.

Applicative Multiprocessing Systems

Principal Faculty

Robert M. Keller
Gary Lindstrom

Affiliated Faculty

Elliott I. Organick
Richard Fujimoto
Thomas C. Henderson
P. A. Subrahmanyam
Tony M. Carter

Staff and Students

8 Ph.D. students
3 M.S. students
1 programmer

Nature of Work

This project entails research on the design and exploitation of distributed computer systems which support applicative (i.e., function-based) languages. Current activity is centered around the development of a multiprocessing system called Rediflow, which is based on a combination of the reduction, data-flow, and von Neumann models of computing. A central feature of this model is its automation of load balancing, which is intended to make it possible for programmers to exploit large-scale multiprocessing without concern for physical placement of tasks within processors and memory.

Current Work Areas

- Language design, including type inference in functional language, multiprocessing pragmas, and the incorporation of logic-programming (e.g., Prolog-like) features into functional languages.
- Applications programming for Rediflow, including logic-programming, databases, knowledge bases, signal processing, and robotics.
- Evaluation of load-balancing and communication network performance via simulation.
- Aspects of physical multiprocessor design.
- Multiprocessor storage reclamation techniques.
- Optimization techniques for applicative multiprocessing, for example, use of data structures which yield greater concurrency.
- Incorporation of indeterminate resource control primitives in an applicative-programming setting.
- Reliability aspects of applicative multiprocessing.

Selected Results

Representative publications are:

1. R. M. Keller, G. Lindstrom, and S. Patil. ''A Loosely Coupled Applicative Multiprocessing System,'' *AFIPS Proc.*, pp. 613-622 (June 1979).

2. R. M. Keller and F. C. Lin. ''Simulated Performance of a Reduction-based Multiprocessor,'' *Computer*, pp. 70-82 (July 1984).

3. A. L. Davis and R. M. Keller. ''Data-flow Program Graphs,'' *Computer*, Vol. 15, No. 2, pp. 26-41 (February 1982).

4. P. Hudak and R. M. Keller. ''Gargage Collection and Task Deletion in Distributed Applicative Processing Systems,'' *Proc. ACM Conf. on LISP and Functional Programming*, pp. 168-178 (August 1982).

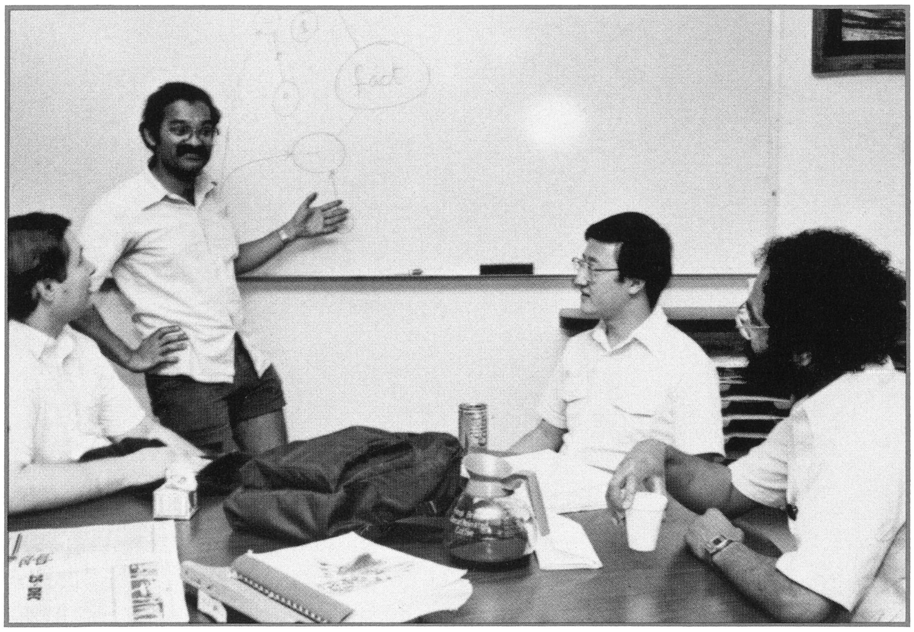
5. B. Jayaraman and R. M. Keller. ''Resource Expressions for Applicative Languages,'' *Proc. IEEE International Conference on Parallel Processing*, pp. 160-167 (August 1982).

Facilities

Current performance of the Rediflow multiprocessor system is being evaluated using a simulator which runs a functional language, FEL. One outcome of such simulations is the derivation of system parameters for ultimate implementation.

Support

The project has received support from the Defense Advanced Research Projects Agency, International Business Machines and the National Science Foundation.



Research on distributed computer systems has resulted in the development of concepts for Rediflow, a multiprocessing system based on the reduction, data-flow and von Neumann models of computing.

Computer Aided Geometric Design

Principal Faculty

Richard F. Riesenfeld
Elaine Cohen
Lewis C. Knapp
Spencer W. Thomas

Staff and Students

2 research scientists
4 Ph.D. students
6 M.S. students

Nature of Work

The Computer Aided Geometric Design Group in Computer Science is involved in both fundamental and applied research in developing methods for representations, specifying and manipulating geometric models in a computer. The group is currently engaged in a concerted effort to develop an advanced geometric modeller that is based on mathematical spline representations. Such work involves research in computer graphics applications to the visualization of complex geometric forms, interfaces to analysis packages, interfaces to manufacturing processes, new design paradigms and user interfaces as well as research into new mathematical surface representations and new geometric algorithms. Challenging test cases are provided by sponsoring agencies which help guide this project and keep it in touch with the practical and fundamental issues that concern design as it occurs in industry.

Current Work Areas

- Developing new mathematical forms for representing freeform surfaces.
- Finding new algorithms for operations on spline-based geometric models, including implementing set operations.
- Studying new CAD/CAM architecture.
- Enhancing and extending computer graphics visualization techniques to help the mechanical designer.
- Exploring new modelling paradigms especially suited for computer implementation.
- Defining appropriate interfaces to the manufacturing process.

Selected Results

- For the past three years, the group has been involved in a concerted effort to build an advanced experimental geometric modeller called Alpha_1 which embodies many theoretical and algorithmic advances.

Representative publications are:

1. E. Cohen, T. Lyche, and R. F. Riesenfeld. ''Discrete Box Splines and Refinement Algorithms,'' submitted for publication (1984).

2. R. F. Riesenfeld. ''A View of Spline-based Solid Modelling,'' *Proc. of Auto-Fact-5* (1983).

3. E. Cohen, T. Lyche, R. F. Riesen-

Specialized graphics equipment includes an Evans and Sutherland Multi-Picture System for producing black and white drawings, and the Grinnell frame buffer and high-resolution monitors for producing color pictures and movies.

feld. "An Application of Discrete B-splines to Computer Aided Geometric Design and Computer Graphics," *Computer Graphics and Image Processing*, Vol. 14, No. 2, pp. 87-111 (October 1980).

4. E. S. Cobb. "Design of Sculptured Surfaces Using the B-spline Representation," Doctoral Dissertation, University of Utah (1984).

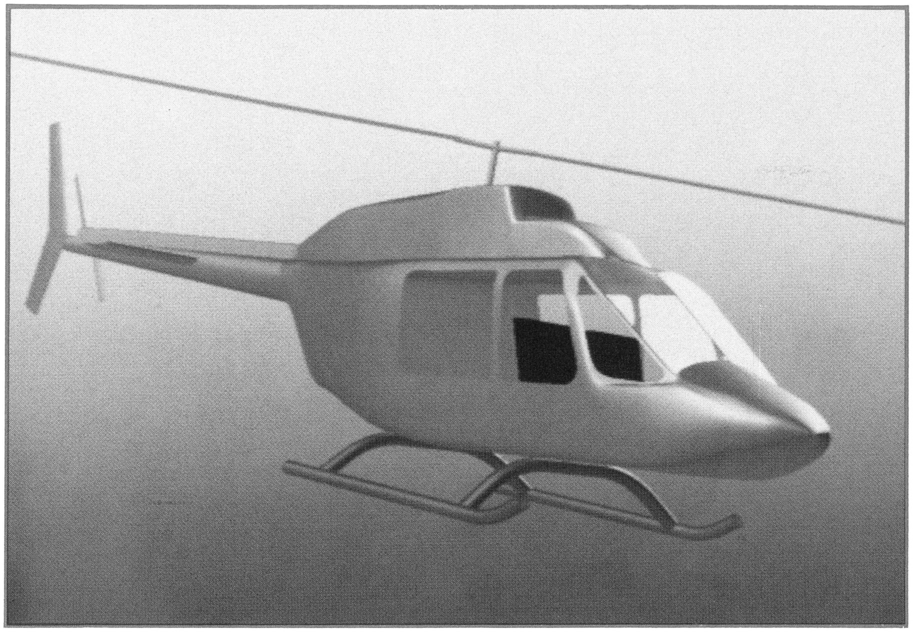
5. S. W. Thomas. "Boolean Operations on Freeform Surfaces," Doctoral Dissertation, University of Utah (1984).

Facilities

The Computer Aided Design and Graphics Laboratory houses a DEC VAX 11/750 as the host computer for many specialized pieces of computer graphics hardware. The VAX has six megabytes of main memory and over a gigabyte of disk space. The specialized graphics hardware currently consists of an Evans and Sutherland Multi-Picture System (MPS) and PS 300 for producing high-resolution black and white line drawings, a Grinnell 512 x 512 frame buffer and several high-resolution color monitors for the production of color pictures and computer generated movies, a Megatek 7290 color raster line-drawing system, and a Lexidata 3D image viewing system. This system also drives a Monarch Cortland 45 Direct Numerical Controlled (DNC) milling machine. Several acquisitions — including a very high resolution (1280 x 1024 x 32 bit) color frame buffer — are in progress. The laboratory also has a Computer-Vision Designer CAD system with two interactive design stations and a Symbolics 3600 LISP Machine. These systems are used for varied computer aided design activities, with emphasis on integrated circuit design and printed circuit board layout. Attached to this system is a very high-speed Calcomp 960 plotter for hard-copy output.

Support

The CAGD group is currently supported by grants, contracts and equipment from the National Science Foundation and the U.S. Department of Defense as well as several private sources.



The CAGD group's current efforts center around developing an advanced geometric modeller based on mathematical spline representations. The results are a system called Alpha_1, which embodies many theoretical and algorithmic advances.

Computer Music

Principal Faculty

Encolino Ferretti

Staff and Students

1 graduate student
2 undergraduate students

Nature of Work

The research in computer music involves the algorithmic representation of composition, performance and instruments for real-time applications, development and implementation of a "Real-time Music Machine" and interdisciplinary education combining technology and music.

Current Work Areas

- Hardware: construction of the Real-time Music Machine, Model 1.
- Software: organization of input data to optimize hardware performance.
- Education: curriculum development combining computing and music as a basis for creative music for students with varying degrees of background in technology and music.

Selected Results

- Programs for synthesizing composition, sounds, performance and instruments.
- Hardware design for a real-time music machine including control structures for parallel processors, pipeline architecture for data routing, fast floating point arithmetic units and special purpose keyboard for real-time performance.
- Three courses in computer music have been developed: Computer Science 565 for computer science majors, Music 451 for music majors and Liberal Education 131 for beginning students with little or no background in either computing or music.

Representative publications are:

1. E. Ferretti. "Parallel Architecture for Real-time Synthesis of Music," *J. Acouti. Soc. Am.*, Suppl. 1, Vol. 66 (Fall 1979).
2. J. A. Stanek. "Exploration of Concurrent Digital Sound Synthesis on a Prototype Data-driven Machine," M.S. Thesis, University of Utah (1979).

Facilities

Computer music facilities include a PDP 11/10 with 16-bit digital-to-analog converter connected to a DECSystem 20 via a serial interface, and a VAX 750 with two 16-bit ADCs and two 16-bit DACs.

Support

Hardware support is currently funded by a University of Utah Research Committee grant. Curriculum development and courses are joint efforts of the departments of computer science, music and liberal education.

Principal Faculty

Elliott I. Organick
Thomas C. Henderson
Gary Lindstrom
P. A. Subrahmanyam

Affiliated Faculty

Robert M. Keller
Thomas G. Stockham Jr.

Staff and Students

5 graduate students
1 staff analyst/programmer

Nature of Work

The main objectives are to integrate use of object-based languages, supporting computer architectures, silicon compilers and other tools for the specification, simulation, test, and evaluation of VLSI circuits realized from high-level language specifications. The language currently under study is Ada, and the host system support architecture for test bed and simulation studies is the Intel 432. Special emphasis is now given to the transformation of signal processing applications to silicon circuits amenable to wafer-level integration.

Computer music research has resulted in the development of a real-time music machine, software support and computer music courses for liberal education, music and computer science students.

Current Work Areas

- Silicon compiler: Software for transforming components specified in Ada to asynchronous circuits in silicon has been under development for more than three years.
- Test bed for designs of chips: The structure and essential behavior of a mixed-level simulator is under study for use in testing program modules under various degrees of concrete representation. These range from a high-level timing-independent form of abstract (soft) representations to gate-level or lower-level timing-specific hardware logic.
- Test bed for chips: Achieving transparent, efficient, and flexible interfaces — between program components realized directly in hardware and those realized through use of conventional machine interpreters (general-purpose host systems) — is regarded as one of the keys to the success of this research. A methodology and the hardware/software support for achieving such interfaces are being developed and tested.

Selected Results

Representative publications are:

1. E. I. Organick, T. M. Carter, M. P. Maloney, et al. ''Transforming an Ada Program Unit to Silicon and Verifying Its Behavior in an Ada Environment: A First Experiment,'' *IEEE Software*, Vol. 1, No. 1, pp. 31-49 (January 1984).

2. E. I. Organick. ''A Programmer's View of the Intel 432 System,'' New York, McGraw-Hill (1983).

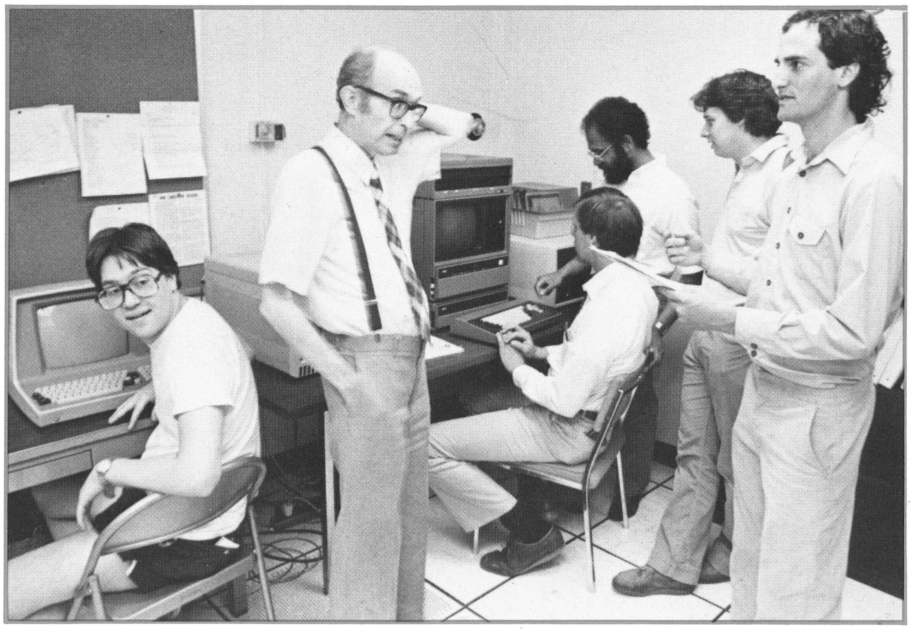
3. P. A. Subrahmanyam. ''Synthesizing VLSI Circuits from Behavioral Specifications: A Very High-level Silicon Compiler and Its Theoretical Basis,'' F. Anceau (editor), *VLSI 83*, International Conference, North Holland (1983).

Facilities

An object-based computing laboratory augments the general computing facilities of the department. This laboratory, centered on a full-scale Intel 432 Cross Development System using Release 3 architecture and software, houses the project's principal physical resource. Cross compiling is accomplished on the department's VAX-UNIX computers which are connected to the development system via the department's local net facility. The laboratory also houses a Lilith computer with laser printer for development of Modula2-based software, which is used for studying the structure of a translator for mapping Modula2 programs into Ada. (This translator is used in programming environments where it is more convenient to develop applications software first in Modula2 and then convert to Ada.)

Support

The laboratory is currently supported by contracts from the Defense Advanced Research Projects Agency and Office of Naval Research, and by smaller grants and contracts from Allied Corporation, Burroughs Corporation, Intel Corporation and Martin Marietta Corporation.



Faculty and graduate students conduct research aimed at transforming signal processing applications to silicon circuits using Ada as a hardware specifiction language.

Portable AI Support System

Principal Faculty

Robert R. Kessler

Staff and Students

3 senior systems programmers
2 part-time technical assistants
3 graduate students
1 undergraduate student

Nature of Work

The Utah Portable AI Support System (PASS) project is developing portable systems capable of supporting AI research and other diverse symbolic computation applications such as algebra, CAGD and VLSI. The portable compiler is the root of portable systems, and research is directed toward showing that a highly optimizing compiler will produce a more productive environment. The key to the system's portability is the incorporation of an architectural description language into all phases of the compiler. This compiler is then used as a "systems programming language" to implement a uniform environment across many different machines; this has been realized in the Utah Portable Standard LISP (PSL) project in which PSL runs on architectures ranging from Motorola 68000s to the Cray XMP. The PASS compiler will initially be for PSL, although there are plans to implement other systems, such as PROLOG, using PSL as the implementation language (much as C might be used as the implementation language). An anticipated result is that much of the work could easily be transferred to another dialect of LISP, such as Common LISP. Emphasizing LISP as the implementation language provides a language that not only operates efficiently in the symbolic world, but also adapts well to "number crunching." PSL will be extended to support datatype analysis at compile time, emphasizing efficient floating point computation to aid applications like the Utah CAGD and VLSI projects.

Current Work Areas

- Architectural description-driven compilation.
- Compiler writing systems.
- Software portability.
- Small-machine LISP and algebra systems.
- LISP system implementation.
- Innovative symbol manipulation methods (hashing, pattern matching, etc.)
- Algebraic manipulation.

Selected Results

PSL (Portable Standard LISP) is the group's most recent LISP system and is recognized as an efficient and portable LISP implementation. PSL is a LISP of about the power and flavor of Franz LISP or MACLISP, with growing influence from Common LISP. The essential ingredients for its success are the writing of a much larger portion of the language in itself than has been done for previous LISP systems, and the development of an optimizing compiler driven by tables describing the target hardware and software environment. PSL has a machine-oriented "mode" for systems programming in LISP (SYSLISP) which permits access to the target machine about as efficiently as in C or PASCAL. As a consequence, PSL has an execution speed comparable to that of Franz LISP (written in C) or MACLISP (kernel hand-coded in assembly code).

The most recent work on PSL has three goals:

- To implement a consistent version of PSL on all departmental machines.
- To improve the efficiency of PSL and the ease with which it is ported to a new target machine.

The Utah Portable Standard LISP runs successfully on architectures ranging from Motorola 68000s to the Cray XMP. The PASS group is currently investigating ways to improve PSL's portability by incorporating an architectural description language into all phases of the compiler.

- To develop a set of significant application programs on PSL and provide a flexible environment for performing the development task.

PSL version 3.1 now runs successfully on the Digital Equipment Corporation's DECSystem 20 and VAX series computers (running Berkeley 4.1 UNIX), the Hewlett-Packard 9836 computer and the Apollo Domain system. All four versions are compatible, allowing software developed on one system to be run directly on any of the others. This systemwide compatibility is the strongest feature of the PSL system.

Representative publications are:

1. M. L. Griss and A. C. Hearn, ''A Portable LISP Compiler,'' *Software Practice and Experience*, pp. 541-605 (1981).
2. M. L. Griss and R. R. Kessler. ''REDUCE 1700: A Microcoded Algebra System,'' *Proc. Micro-11*, pp. 130-138 (1978).
3. M. L. Griss, E. Benson and G. Q. Maguire Jr. ''PSL: A Portable LISP System,'' *Proc. of the 1982 ACM Symposium on LISP and Functional Programming*, pp. 88-97 (1982).
4. R. R. Kessler. ''PEEP — An Architectural Description-driven Peephole Optimizer,'' *Proc. of the Sigplan 1984 Symposium on Compiler Construction*, to appear (1984).
5. R. R. Kessler, H. Carr, W. Galway, J. Krohnfeldt and B. Othmer. ''A Portable Typed LISP Compiler Based on an Architectural Description Language,'' *Utah PASS Opnote 84-01 (1984).*

Facilities

The main computing activity of the group is centered on the department's DECSystem 2060, VAX 750s, Apollo Domain nodes and Hewlett-Packard 9836 workstations.

Support

The research activities of the group have been funded by several agencies with the principal support coming from the National Science Foundation and many industrial concerns.

Robotics and Computer Vision

Principal Faculty

Bir Bhanu
Thomas C. Henderson

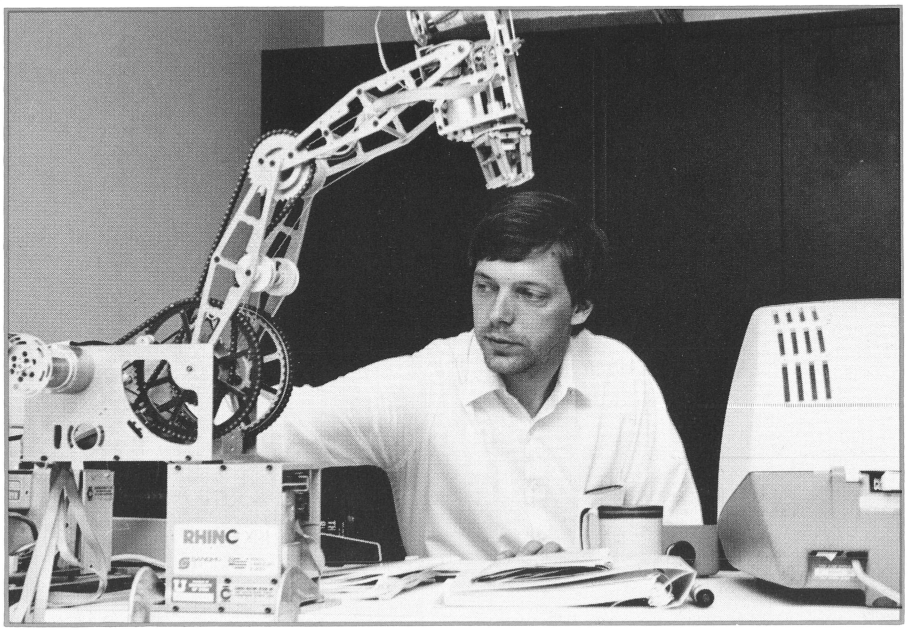
Staff and Students

2 graduate students
4 undergraduate students

Nature of Work

The research program is directed toward solving both practical and theoretical problems in robotics, vision and sensory control. The design and development of complete robotic systems are of central concern as are individual components of such systems. In particular, the group is studying high-level control of a multifingered robot hand, contact sensors for the hand, image processing and pattern recognition aspects of the robot hand, multi-sensor integration systems, 3D sensing systems, representations and modelling of objects, computation of salient grasping and manipulation features, and industrial tasks.

A major area of work is computer aided geometric design (CAGD)-based computer vision tor recognition and manipulation of 3D objects. Work also is progressing on the segmentation, classification and contextual cueing algorithms, and on the evaluation of various image processing and pattern recognition algorithms and expert systems.



Robotics research is facilitated by several robots including the group's Rhino XR-1 six-degree-of-freedom robot arm. Work of the group is supported by NSF and the Army Research Office.

Current Work Areas

- CAGD-based vision analysis.
- Low-level representations of sensor data.
- Logical sensor specification and multisensor integration.
- Representation and models of 2D and 3D objects.
- Constraint-based analysis.
- Evaluation of pattern recognition and image analysis algorithms.
- Contextual cueing, expert systems.
- Multifingered hand control using vision and tactile sensors.
- Robot hand grasping and manipulation strategies.
- Robot-task specifications.

Selected Results

Representative publications are:

1. B. Bhanu. ''Representation and Shape Matching of 3D Objects,'' IEEE Transactions on Pattern Analysis and Machine Intelligence, *PAMI-6*, pp. 340-351 (May 1984).

2. B. Bhanu and O. D. Faugeras. ''Shape Matching of Two-dimensional Objects,'' IEEE Transactions on Pattern Analysis and Machine Intelligence, *PAMI-6*, pp. 137-156 (March 1984).

3. B. Bhanu and O. D. Faugeras. ''Segmentation of Images Having Unimodal Distributions,'' IEEE Transactions on Pattern Analysis and Machine Intelligence, *PAMI-4*, pp. 408-419 (July 1982).

4. B. Bhanu and J. H. McClellan. ''On the Computation of Complex Cepstrumm,'' IEEE Transactions on Acoustics, Speech, and Signal Processing, *ASSP-28*, pp. 583-585 (October 1980).

5. T. C. Henderson and E. Triendl. ''Storing Feature Descriptions as 2D Trees,'' *Proc. of IEEE Conference on Pattern Recognition and Image Processing*, pp. 555-556 (June 1982).

6. T. C. Henderson and S. F. Wu. ''A Multisensor Integration and Data Acquisition System,'' *Proc. of IEEE Conference on Computer Vision and Pattern Recognition*, pp. 274-279 (June 1983).

7. T. C. Henderson. ''Efficient 3D Object Representations for Industrial Vision Systems,'' Special issue of *IEEE Transactions on Pattern Analysis and Machine Intelligence*, pp. 609-618 (November 1983).

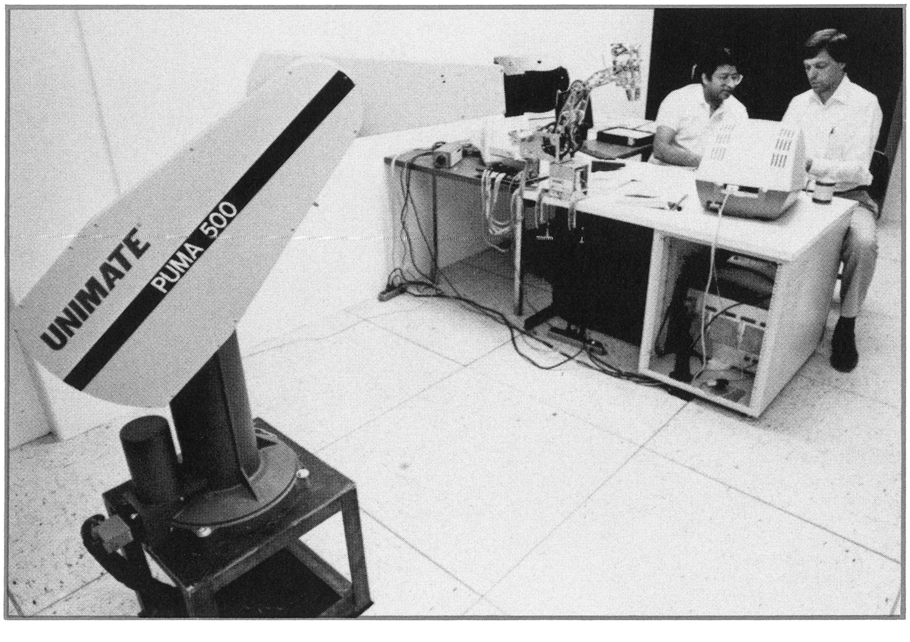
8. T. C. Henderson, C. Hansen, E. Shilcrat, and S. F. Wu. ''Logical Sensor Specifications,'' *Proc. of SPIE Conference on Intelligent Robots*, pp. 578-583 (November 1983).

Facilities

In addition to a VAX 11/750 and graphics facilities, the computer vision and robotics group has a Rhino XR-1 six-degree-of-freedom robot arm, a Unimate PUMA 560 six-degree-of-freedom arm, and a laser range-finder White scanner. The graphics facilities provide a suitable environment for simulations, and the Mechanical Engineering Department's Center for Biomedical Design complements the research of the robotics group by allowing first-hand experience with the latest in robotics technology such as the multi-fingered hand. The group is acquiring a vision system, grippers and other lab accessories.

Support

Computer vision and robotics research is supported by grants from the National Science Foundation and the Army Research Office.



The Unimate PUMA 560 six-degree-of-freedom arm is the focus of much of the robotics group's work with robot task specifications as well as grasping and manipulation strategies.

Text Retrieval

Principal Faculty

Lee A. Hollaar

Affiliated Faculty

Kent F. Smith

Staff and Students

2 Ph.D. students
7 M.S. students
2 staff programmers

Nature of Work

The Utah Text Retrieval Project seeks well-engineered solutions to the implementation of large (more than 50 million characters), inexpensive (less than $1 per query), rapid (average response time of ten seconds) text information retrieval systems. The project has three major components. Perhaps the best known is the work on the specialized processors, particularly search engines, necessary to achieve the desired performance and cost. The other two concern the user interface to the system and the system's internal structure.

The work on user interface development concentrates not only on the syntax and semantics of the query language, but also on the overall user environment. Environmental enhancements include convenient ways to "browse" through retrieved documents, access to other information retrieval systems through gateways supporting a common command interface, and interfaces to word processing systems. The system's internal structure is based on a high-level data communications protocol linking the user interface, index processor, search processor, and other system modules. This allows them to be easily distributed in a multi- or specialized-processor configuration. It also allows new modules, such as a knowledge-based query reformulator, to be added.

Also being studied is the use of more conventional, structured databases and the extensions necessary to support VLSI design techniques. A relational database system, enhanced to support the hierarchically structured data common to cell-based designs, has been developed emphasizing the user interface and storage requirements. A demonstration implementation is planned for a centralized database server on the departmental workstation network.

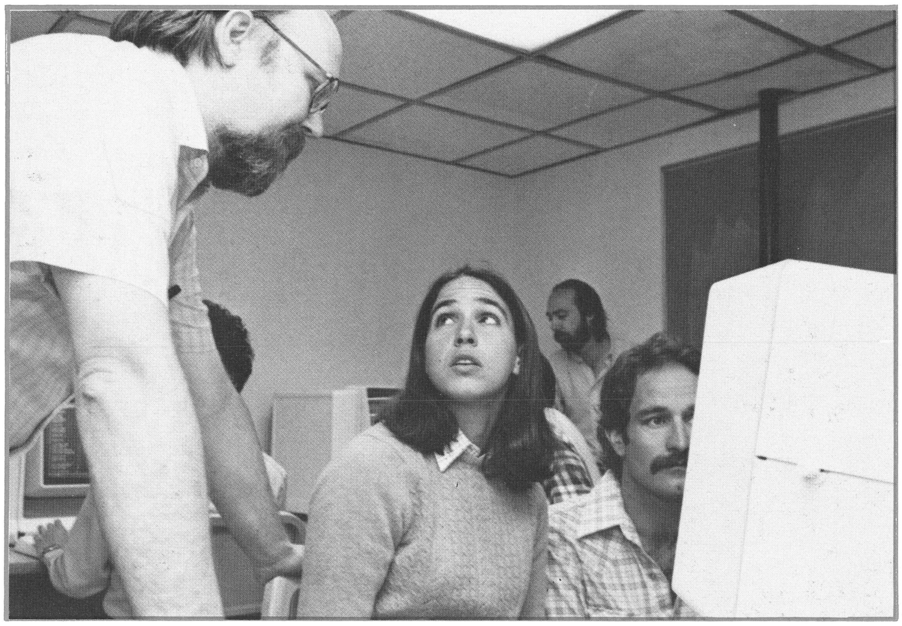
Current Work Areas

- Development of the prototype of the text search engine.
- Implementation of a demonstration text retrieval workstation with window management and document processing facilities.
- Determination of system design parameters and performance for a variety of actual applications.
- Implementation of a VLSI design database management system.

Selected Results

Representative publications are:

1. L. Hollaar. "The Utah Text Retrieval Project," *Information Technology: Research and Development*, Dublin (1983).
2. L. Hollaar, K. Smith, W. H. Chow, R. Haskin, and P. Emrath. "The Architecture and Operation of a Large, Full-text Information Retrieval System," International Workshop on Database Machines (August 1982); also in *Advanced Database Machine Architecture*, Prentice-Hall (1983).
3. R. Haskin and L. Hollaar. "Operational Characteristics of a Hardware Pattern Matcher," *ACM Transactions on Database Systems* (March 1983).
4. L. Hollaar. "Specialized Merge Processor Networks for Combining Sorted Lists," *ACM Transactions on Database Systems* (September 1978).
5. L. Hollaar. "Text Retrieval Computers," *Computer* (March 1979).



The Text Retrieval project has three major components—work on specialized processors, the user interface to the system and the system's internal structure. Emphasis is on text retrieval systems that are large, inexpensive to use and quick.

Video-computer Courseware Implementation System

Facilities

The project is a major user of the departmental computer facilities, including the VAX-UNIX and DECSystem 20. The demonstration text retrieval system is being implemented on the Apollo Domain workstation network. The project also has a number of IBM Personal Computers and a Compaq. The development of the text search processor custom VLSI circuit is being done using the ComputerVision system, with prototype fabrication in the HEDCO Microelectronics Laboratory.

Support

The development of the text search engine has been supported by the National Science Foundation. Development of the information retrieval system has been supported by NSF and other government agencies as well as Digital Equipment Corporation. The design of the VLSI design database system was supported by the NSF and International Business Machines.

Principal Faculty

Richard Brandt
P. A. Subrahmanyam
Nancy Coldeway (Education)

Staff and Students

Barbara H. Knapp, Project Co-Director
3 M.S. students (Computer Science)
14 undergraduate students

Nature of Work

The Video-computer Courseware Implementation System (VCIS) group is developing tools for implementing and authoring courseware on microcomputers. The group is currently investigating issues involving transportability of courseware and software, human-computer interface issues in computer-based instruction, quality control for computer-based instruction, and the use of artificial intelligence in computer-based instruction.

Current Work Areas

- Development of authoring and implementation tools for the UNIX environment.
- Development of software and courseware portability strategies for small machines.
- Transportation of the VCIS software (currently running on Terak and HP microcomputers) to the VAX series and the 8088 series (Zenith Z-100, IBM PC).
- Development of computer aided instructional systems using associative networks.

Selected Results

Representative publications are:

1. R. C. Brandt and B. H. Knapp. "Interactive Videodisc Authoring Concepts," Chapter 4, *Videodisc / Microcomputer Courseware Design*, Michel L. Debloois (editor), Educational Technology Publications (1982).
2. B. H. Knapp and R. C. Brandt. "Video-computer Courseware Implementation System User's Manual," University of Utah (1983).
3. R. C. Brandt. "Interactive Video in Engineering Education," *Proc. FIE Conf.*, Worcester (October 1983).
4. R. C. Brandt. "Courseware Transportability Issues," ADCIS 82: Computer Literacy, Intelligent CAI (June 1982).

Undergraduates and graduate students play an important role in the work of the VCIS group, which is developing tools for implementing and authoring courseware on microcomputers. Central to the investigation is the portability of software and courseware for small machines.

Very Large Scale Integration

Facilities

The Video-computer Learning Laboratory contains several Terak 8510a microcomputers and a Terak 8600 color display system with color overlay on video, one Hewlett-Packard 9836 microcomputer, two Z-100 microcomputers, two IBM PCs, two Tandy TRS 80 Model 2000s, five color graphics terminals, one black and white graphics terminal, a TI microcomputer, and a laser videodisc player.

Support

This project is principally funded by the U.S. Navy through the Naval Personnal Research and Development Center (NPRDC). The U.S. Naval Research Laboratory is funding the movement of the VCIS programs to the VAX computers. All but one of the computers in the laboratory were donated or loaned by industry.

Principal Faculty

Kent F. Smith
Tony M. Carter

Affiliated Faculty

Lee A. Hollaar
Robert Huber (Electrical Engineering)

Staff and Students

2 systems programmer/analysts
4 Ph.D. students
5 M.S. students

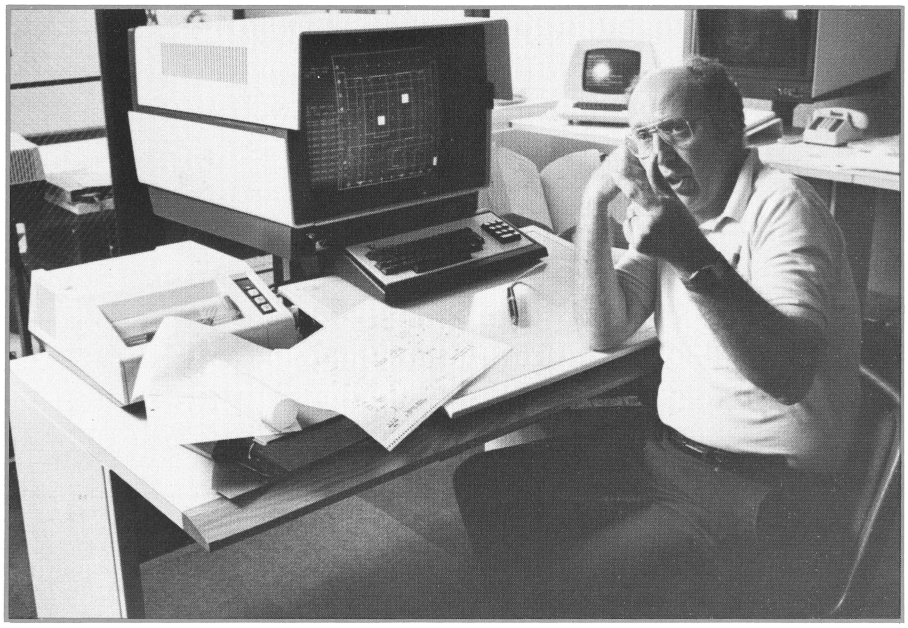
Nature of Work

The VLSI group is currently working on several board areas including: NMOS and CMOS implementations of Structured Tiling, low-cost CAD for VLSI (CAD tools which run on personal computers), high-level CAD tools for VLSI design (approaching the Silicon Compiler), structured methods for designing arithmetic integrated circuits, self-timed and asynchronous machines, relational database-oriented CAD systems for VLSI design, and a VLSI implementation of a database search machine.

The group is simplifying CAD development by using appropriately structured integrated circuit design techniques, hiding much of the low-level detail from the design and the CAD developer.

Current Work Areas

- NMOS implementation of Path-programmable Logic.
- CMOS implementation of Path-programmable Logic.
- Automatic implementation of self-timed and asynchronous finite automata.
- PPL design tools (editors, simulators, etc.)
- Critical path analysis for Path-programmable Logic.
- Compaction of Path-programmable Logic circuits.
- NMOS and CMOS implementation of Structured Arithmetic Tiling.
- Automating the design and implementation of complex arithmetic circuits.
- Testing of self-timed and asynchronous finite automata.
- Testing of Path-programmable Logic circuits.



The VLSI group has developed a method for fast design of integrated circuits. These techniques involve both software packages and integrated circuit hardware.

Selected Results

The following packages are fully operational or well into development:

- PPL — a structured IC design method for random logic and RTL design.
- SAT — Structured Arithmetic Tiling, a structured IC design method for arithmetic circuits.
- SLED — a PPL editor running on a wide variety of machines.
- ASYLIM — a PPL simulator running on a wide variety of machines.
- ASSASSIN — an automatic, self-timed, finite automata compiler.
- MASHER — an automatic PPL circuit compactor.
- ULC — a translator system for converting IC layouts between various representations.

Representative publications are:

1. K. F. Smith, T. M. Carter, and C. E. Hunt. "Structured Logic Design of Integrated Circuits Using the Stored Logic Array," *IEEE Transactions on Electronic Devices*, Vol. ED-29, No. 4, pp. 765-776 (April 1982).

2. T. M. Carter and L. A. Hollaar. "The Implementation of a Radix-16 Digit-Slice Using a Cellular VLSI Technique," *Proc. of the 1983 IEEE International Conference on Computer Design/VLSI in Computers*, pp. 688-691 (November 1983).

3. T. M. Carter. "ASSASSIN: A CAD System for Self-timed Control-unit Design," IEEE Transactions on Computer Aided Design for Integrated Circuits and Systems, accepted for publication.

4. K. F. Smith. "Design of Regular Arrays Using CMOS PPL," *Proc. of the 1983 International Conference on Computer Design/VLSI in Computers*, pp. 158-161 (November 1983).

Facilities

The VLSI group uses the departmental computing facilities extensively and also has several Apollo Domain workstations and four IBM PC-XTs. The testing lab consists of a Hewlett-Packard 9836 computer for controlling a variety of equipment including an HP4145 parameter extractor, HP4275 LCR meter, Tektronix DAS-9000 logic analyzer with 48 channels of generation and 64 channels of acquisition, and a Pacific Western probe station.

The group has a ComputerVision CGP-200 system running CADDS2/VLSI. This system consists of a processing unit, 134 megabyte disk drive, two storage-tube displays, one color raster display, and a Calcomp 960 plotter. The system also shares a Versatec printer/plotter with the graphics group. A Symbolics 3600 LISP Machine has been acquired for use in the development of a silicon compiler.

Facilities of the HEDCO Microelectronics Laboratory are available for fabricating circuits. Some projects have also used the lab for special processes not available in industry.

Support

The research is currently funded by DARPA, the National Science Foundation, International Business Machines and General Instrument Corporation.

VLSI laboratory equipment includes a ComputerVision CGP-200 system with a Calcomp 960 plotter. Researchers also have access to extensive departmental computing facilities as well as the HEDCO Microelectronics Laboratory's specialized equipment for fabricating circuits.

University of Utah
Department of Computer Science
3160 Merrill Engineering Building
Salt Lake City, Utah 84112